

1~3	Cover Sheet /System Block Diagram /Clock Distribution
4	CPU-CNTL/CLK/MISC/FDI
5	CPU-Memory
6	CPU-Power
7	CPU-GND
8	DDR III DIMM 1 / DIMM 2
9	DDR III DIMM 3 / DIMM 4
10	PCH-PCI/E/DMI/USB
11	PCH-CLK
12	PCH-PCH-VGA/FDI/USB30
13	PCH-SATA
14	PCH-SMB/LPC/AUDIO/RTC
15	PCH-STRAP
16	PCH-POWER
17	PCH-GND
18	SIO-Fintek/F71889AD LAC
19 20	PCIE x16 and x1 Slots /PCIE X8
21	LAN - RTL8111E-VL-CG
22	Audio Codec ALC892-CG
23	eSATA - Asmedia 1061
24	FAN
25 26	Rear/Front USB Connectors /power
27 28	USB3.0-Real /Front Port
29	ATX F_Panel/EMI/LED
30	XDP/ USB PW-Discharge
31	ACPI
32	PCH Core Power
33	CPU_VTT
34	VCC_SA POWER
35	DDR Power
36	VRD12- 6+1 Phase PWM ISL6366
37	VCCP MOS
38	GFX MOS
39	HDMI
40	D-SUB
41	EMI
42	Manual & Option parts

# MS-7785M1 Version : 11

**CPU :**  
**INTEL Ivy Bridge Processor**

**System Chipset :**  
**INTEL Panther Point Chipset**

**On Board Chipset :**

**VRM 12 -- ISL6366CRZ-T 6+1 Phase**

**Gigabit LAN -- RTL8111E-VL-CG**

**HDA Codec -- Realtek ALC892-CG**

**Super I/O -- Fintek/F71889AD LAC**

**SPI Flash 64Mb**

**Main Memory :**

**2 Channel DDR III \* 4 (Max 32GB)**

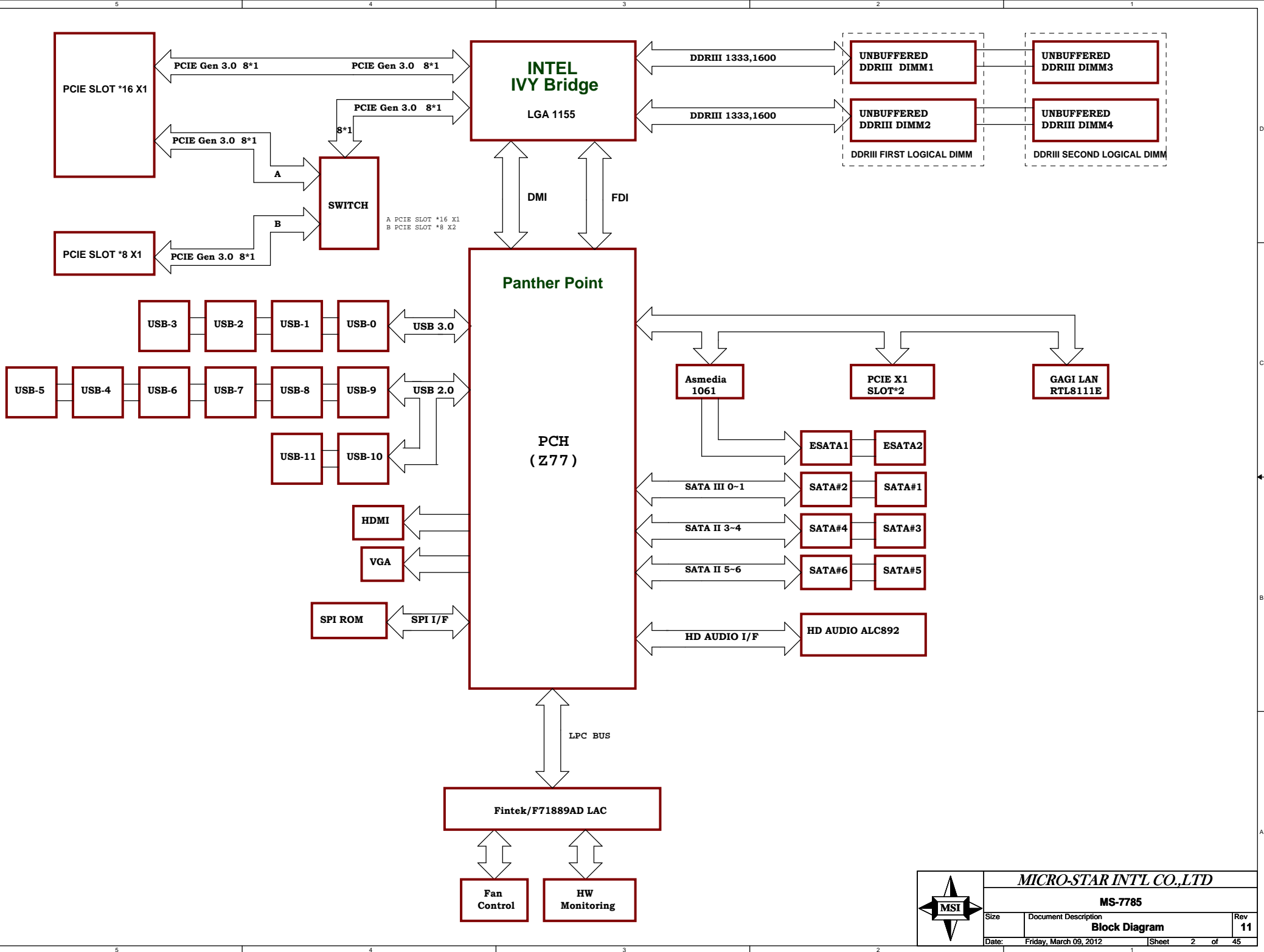
**Expansion Slot :**

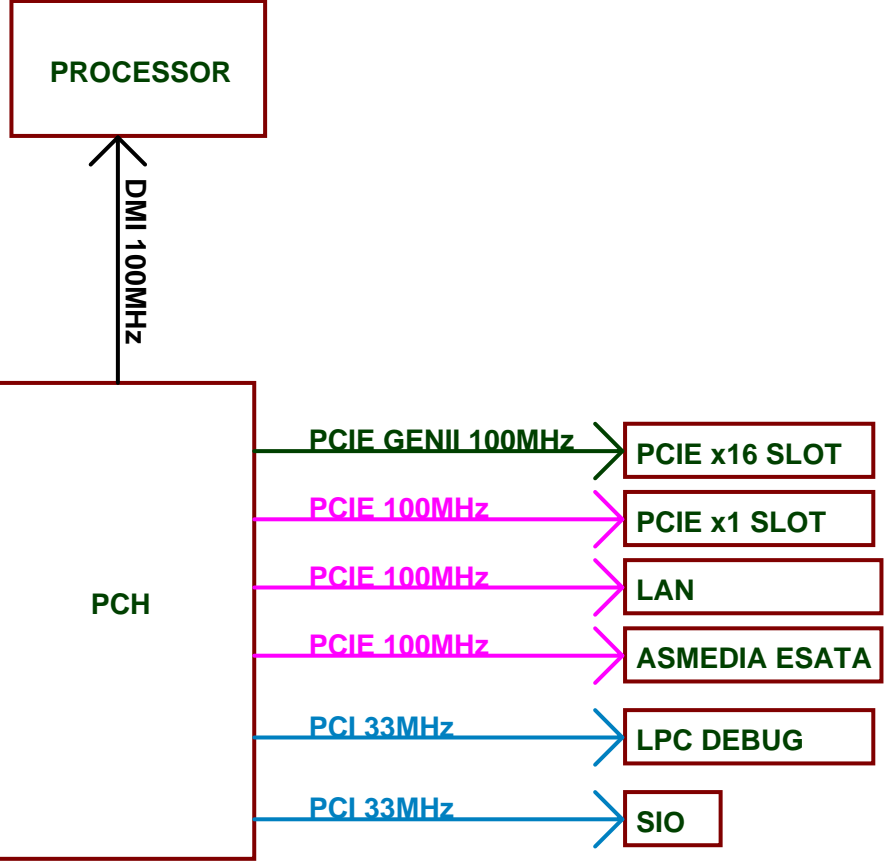
**PCI Express x16 Slot \* 2**

**(16X Gen3 \* 1 or 8X Gnen 3 \* 2 )**

**PCI Express x1 Slot \* 2**



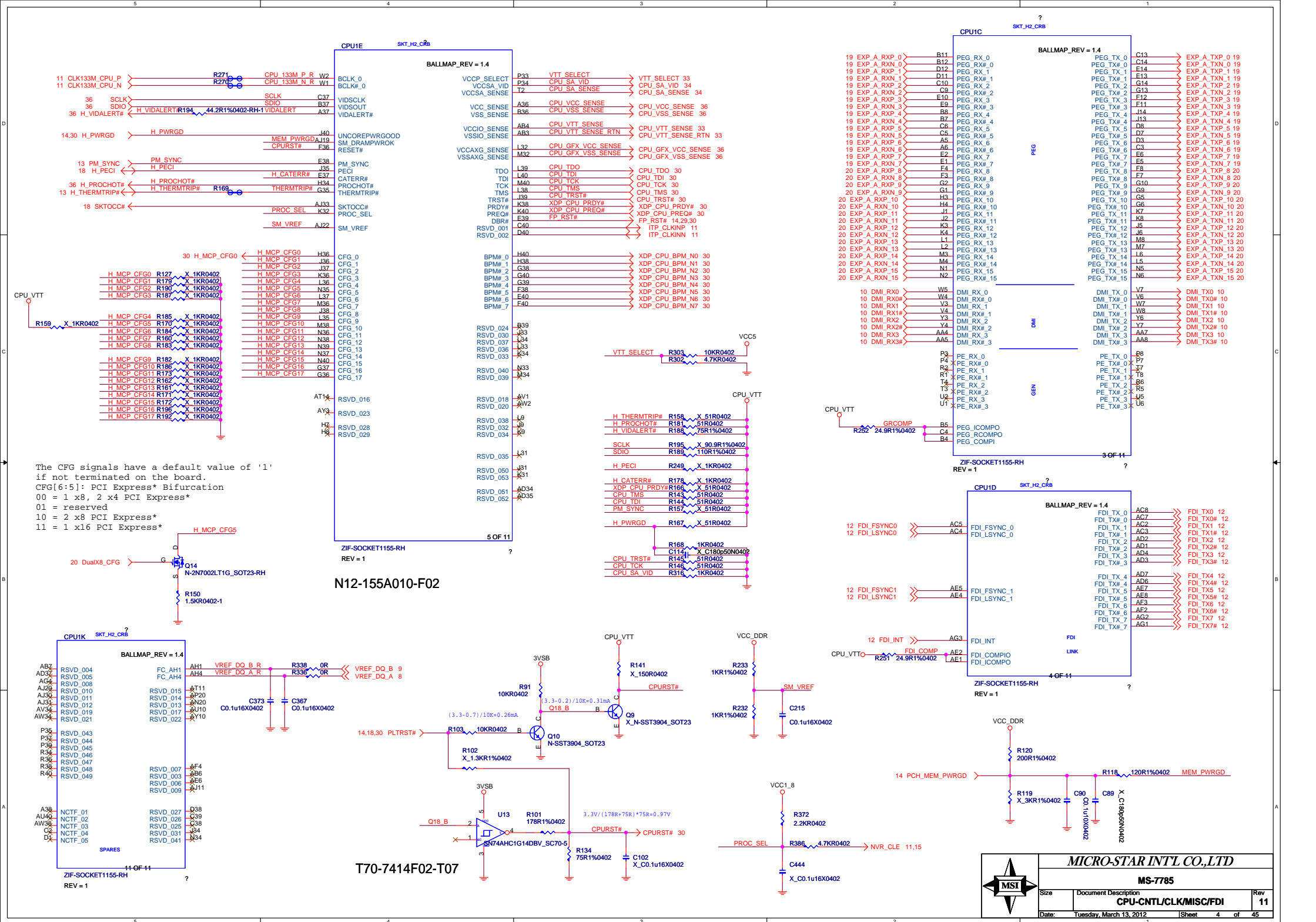


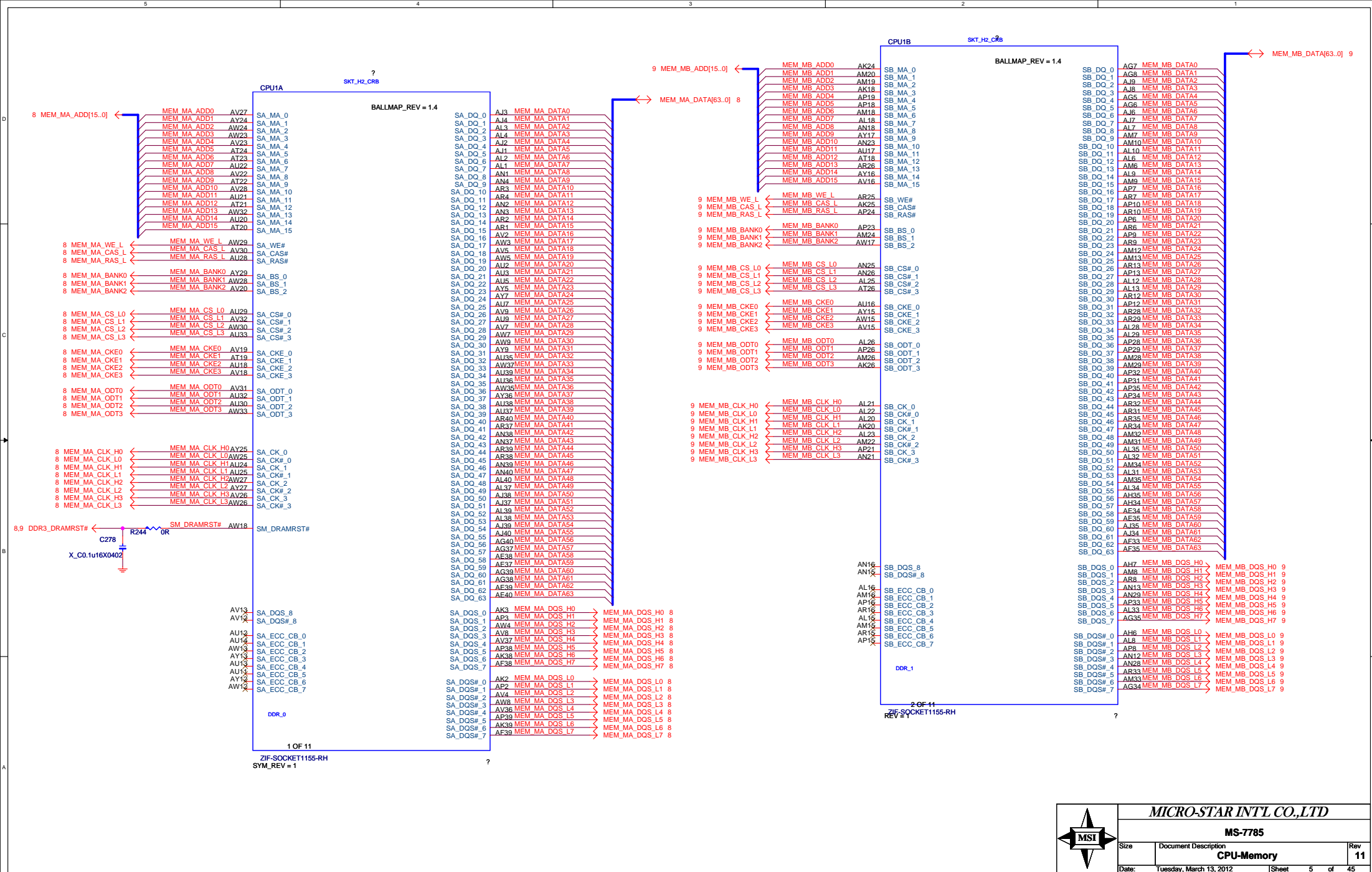


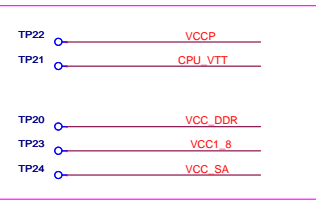
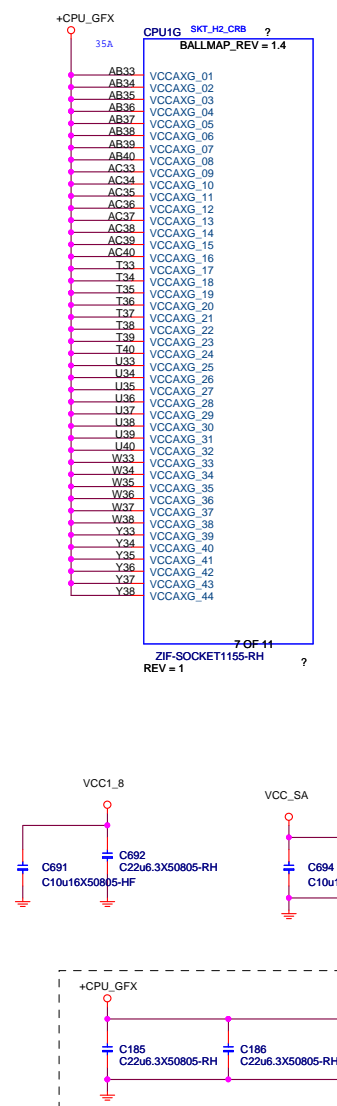
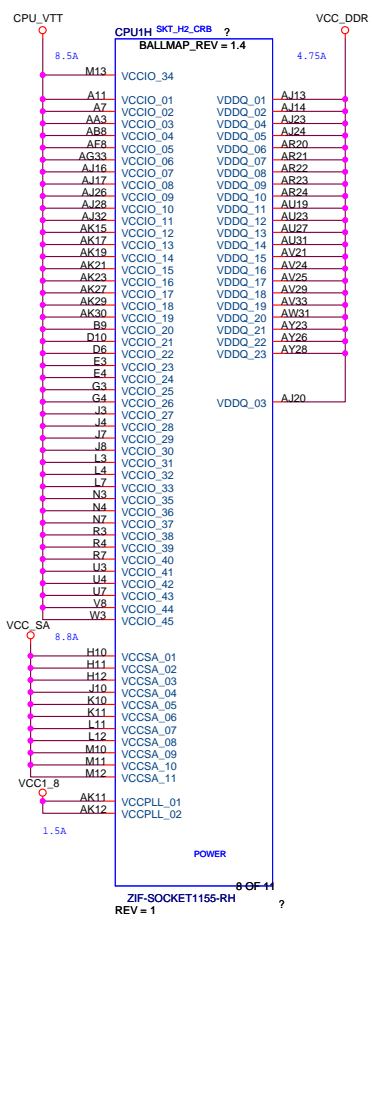
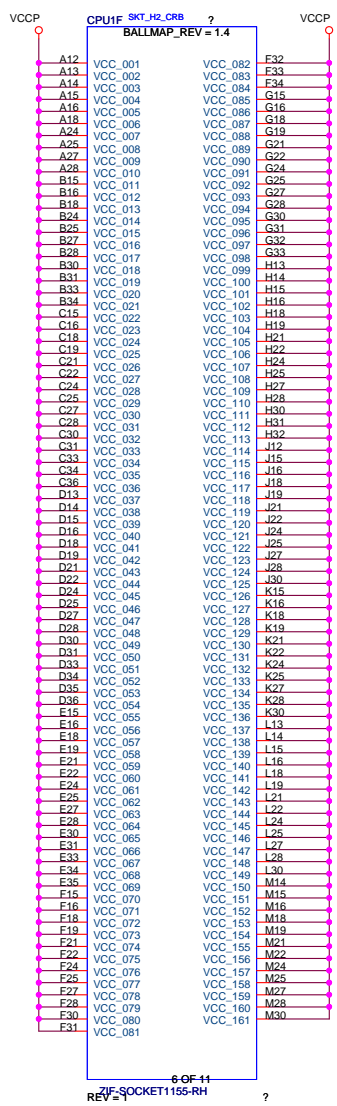
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MS-7785

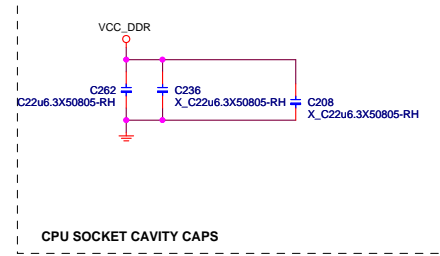
Size	Document Description	Rev
	Clock Distribution	11
Date:	Friday, March 09, 2012	Sheet 3 of 45



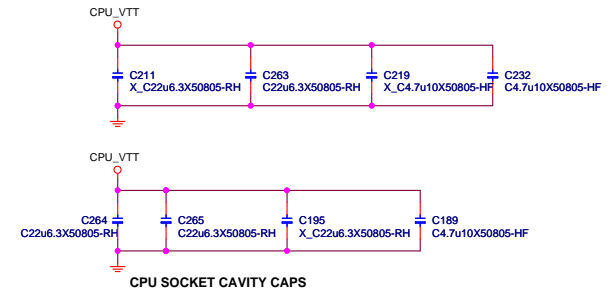




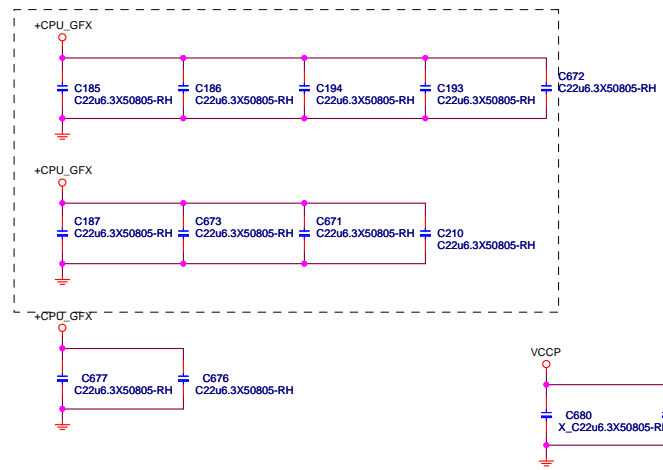
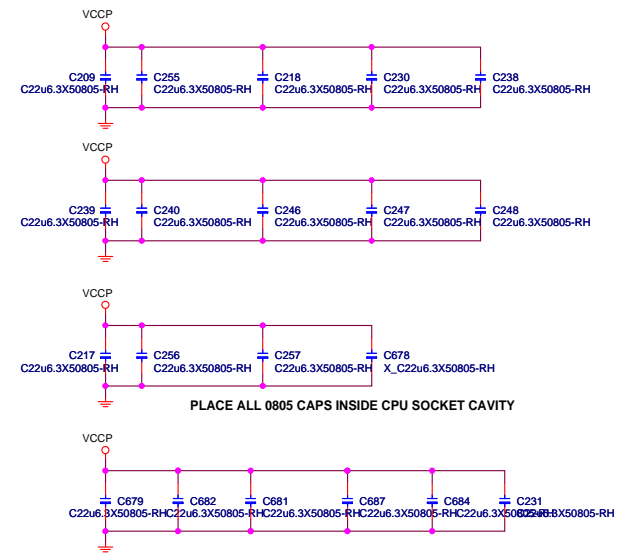
### +1.5V\_DDR3-Decoupling

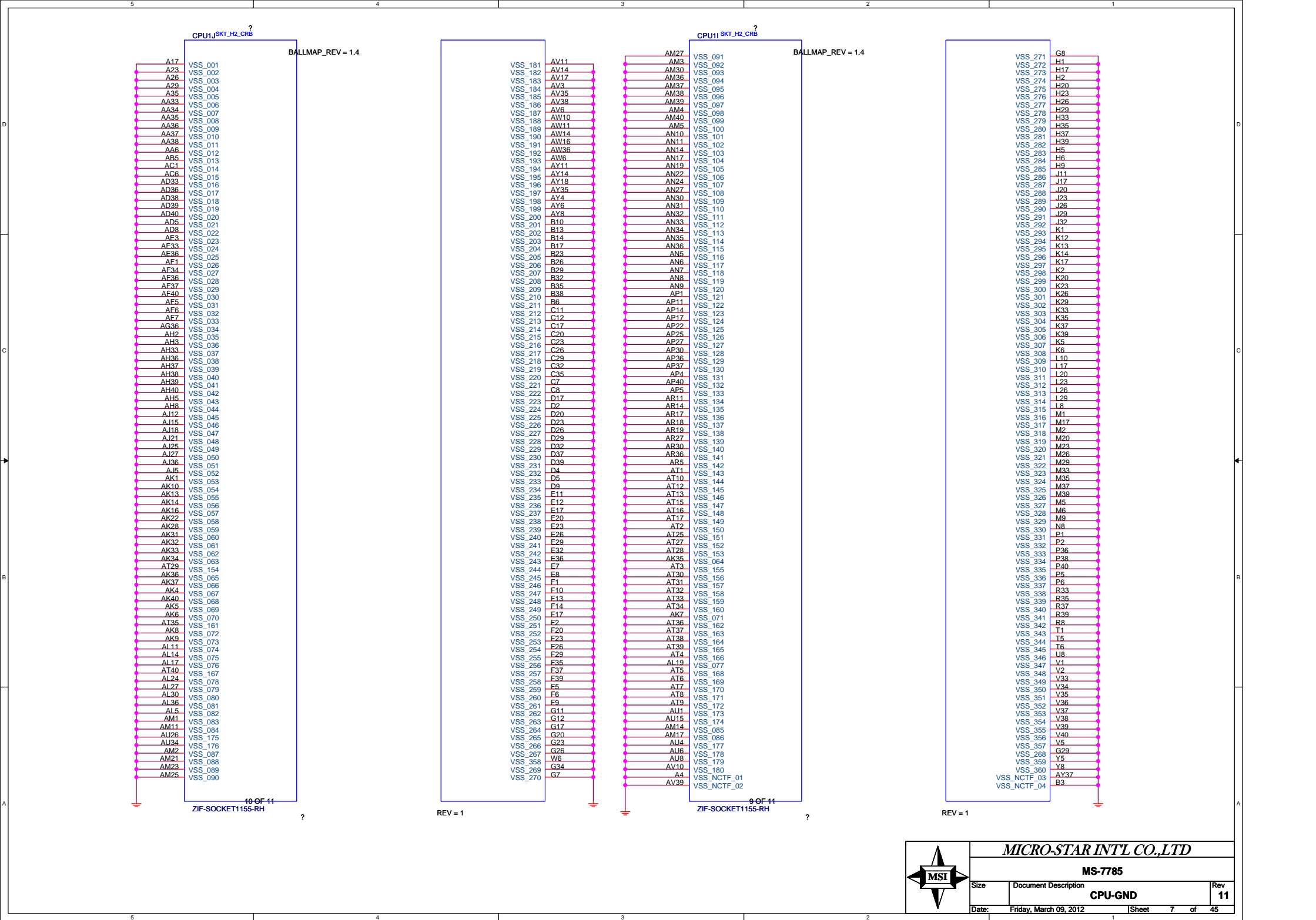


### +CPU\_VTT Decoupling



### +CPU\_VCCP-Decoupling





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Size Document Description Rev

CPU-GND

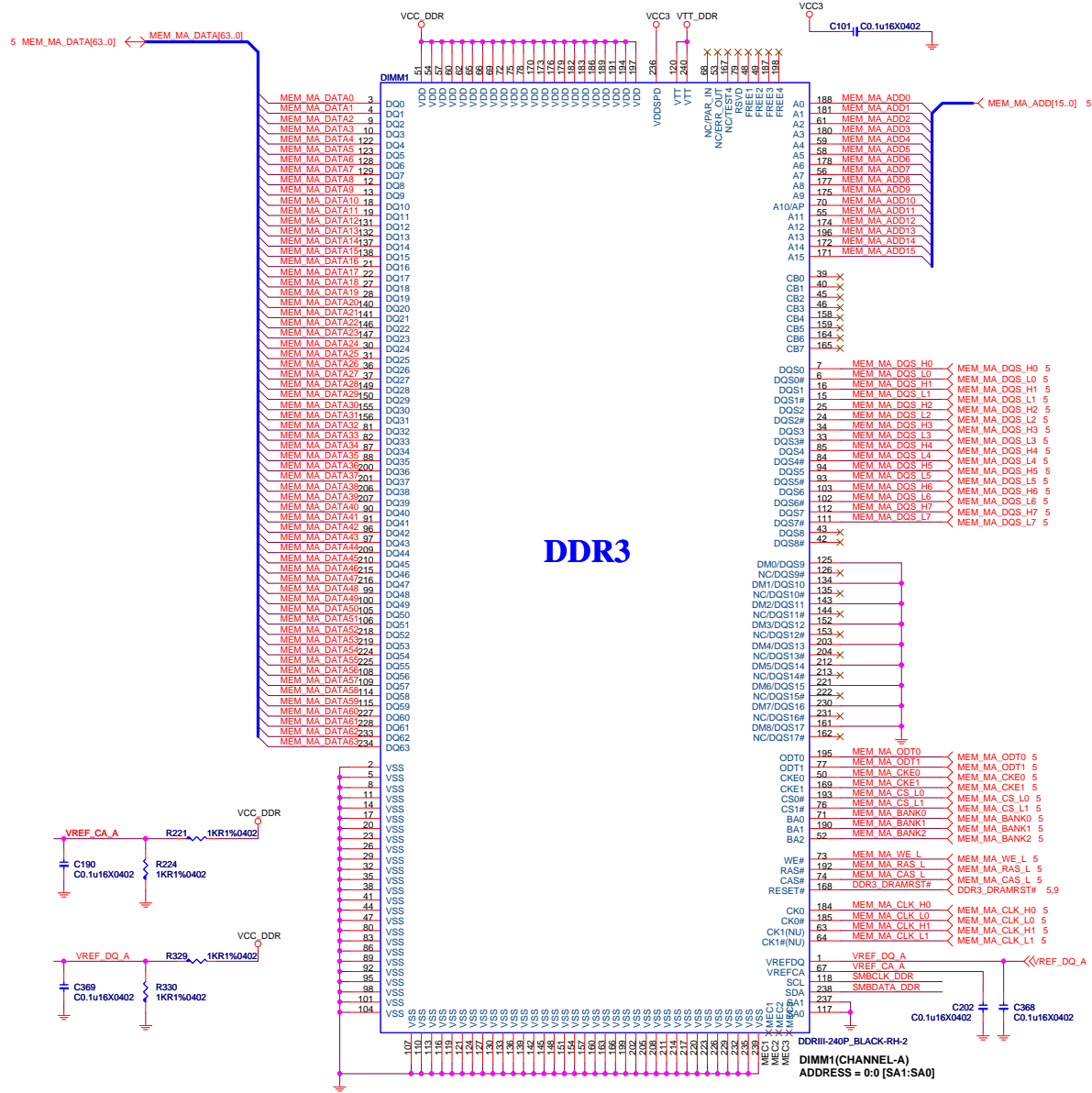
11

Date: Friday, March 09, 2012 Sheet 7 of 45

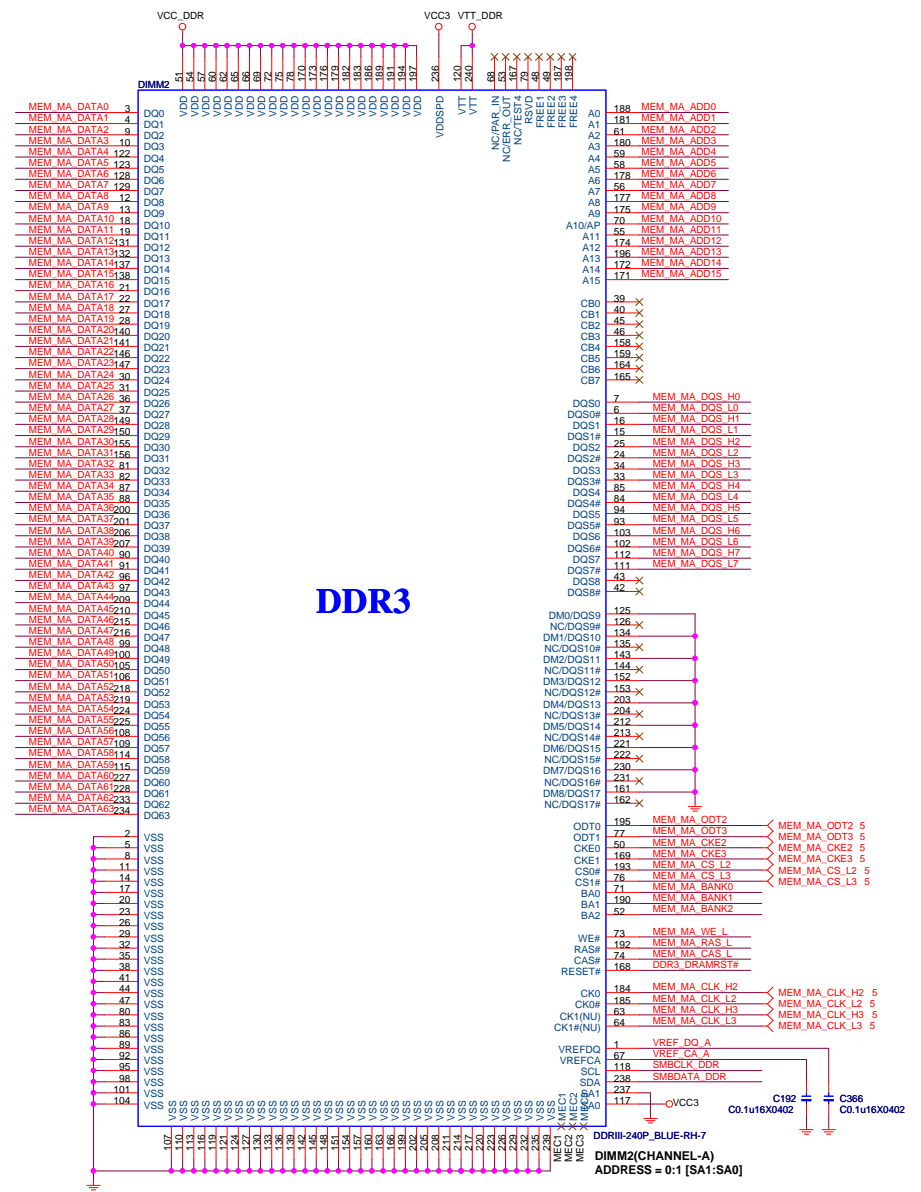


## DDR3 DIMM\_A1

## DDR3 DIMM\_A2



N13-2400601-K06



N13-2401121-K06

9 SMBCLK\_DDR ← SMBCLK\_DDR R97 33R0402 → SMB\_CLK\_MAIN 14,30,33,36  
9 SMBDATA\_DDR ← SMBDATA\_DDR R105 33R0402 → SMB\_DATA\_MAIN 14,30,33,36

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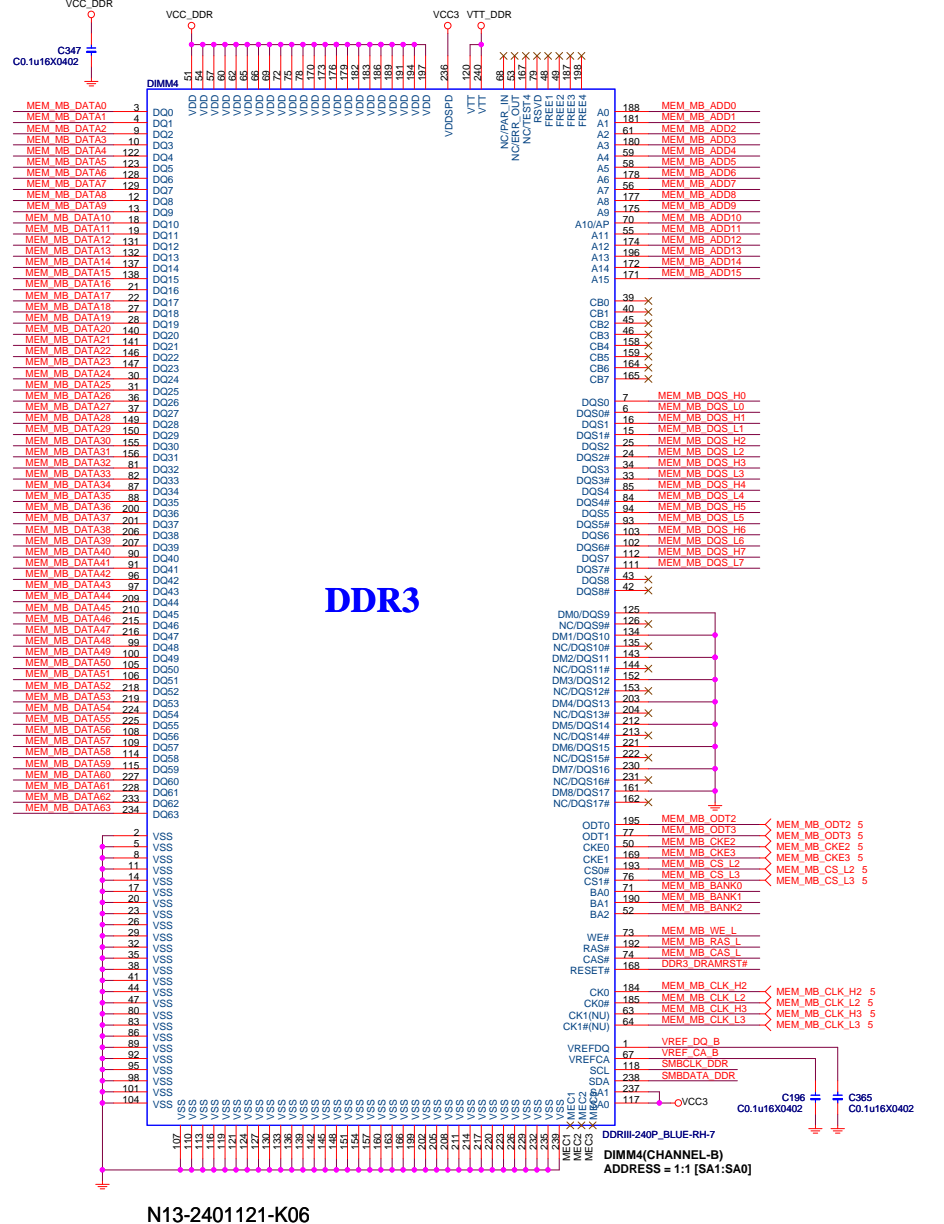
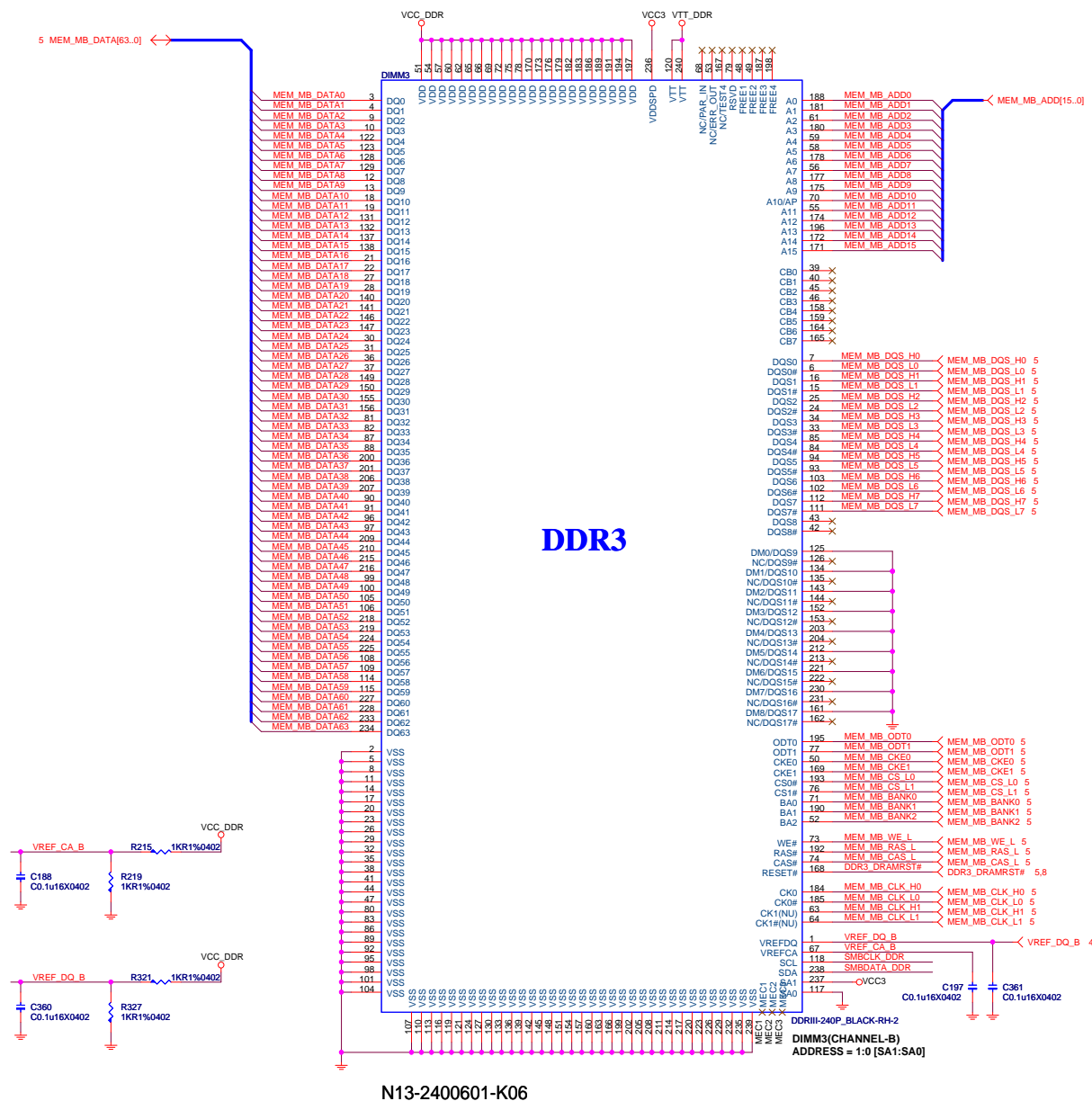
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# DDR3 DIMM\_B1

# DDR3 DIMM\_B2



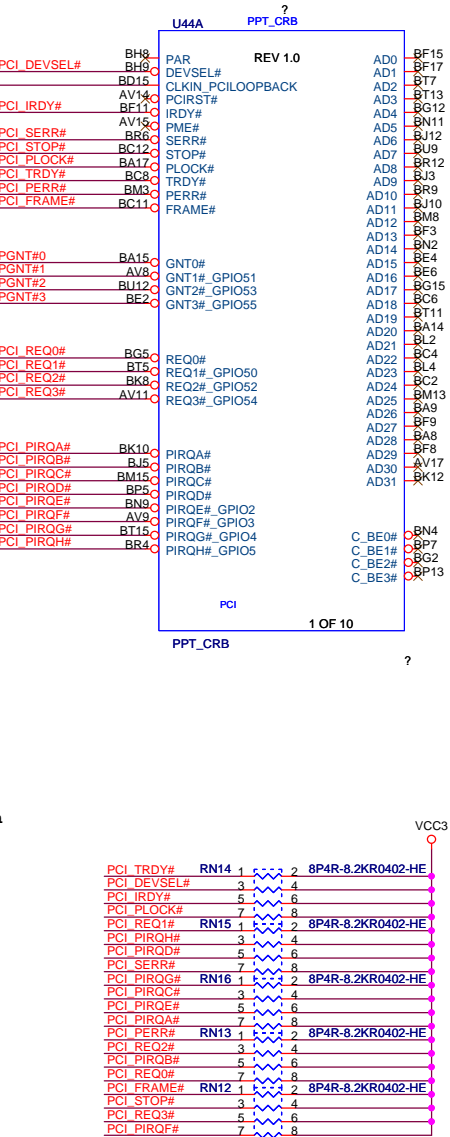
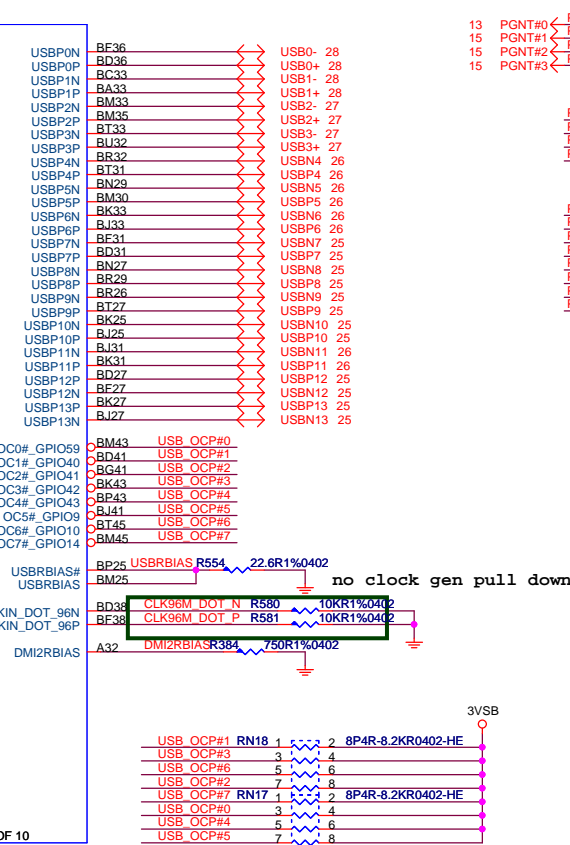
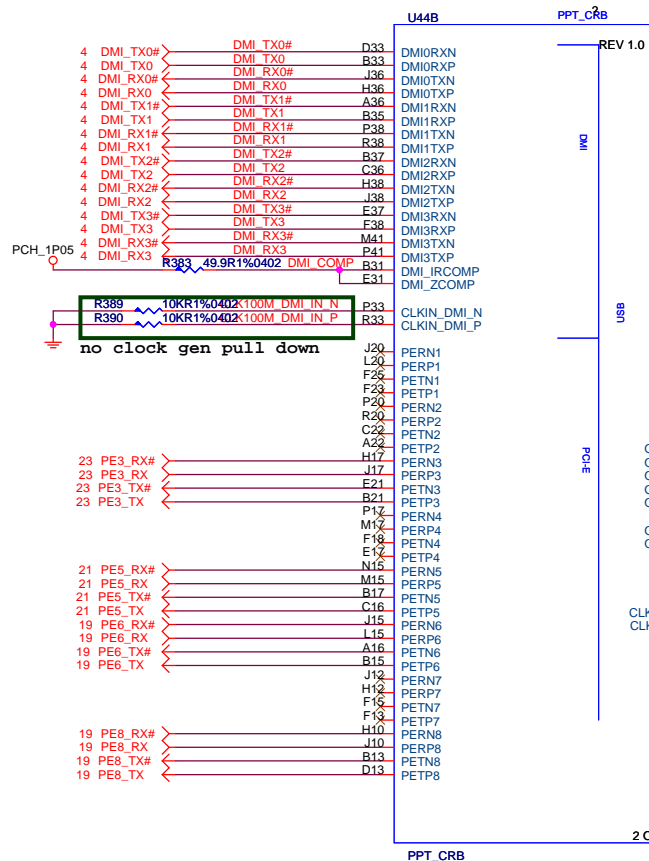
N13-2400601-K06

N13-2401121-K06

SMBCLK\_DDR < SMBCLK\_DDR 8  
SMBDATA\_DDR < SMBDATA\_DDR 8



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MS-7785			
Size	Document Description	Rev	
1	DDR3 Chane1-B DIMM3/4	11	
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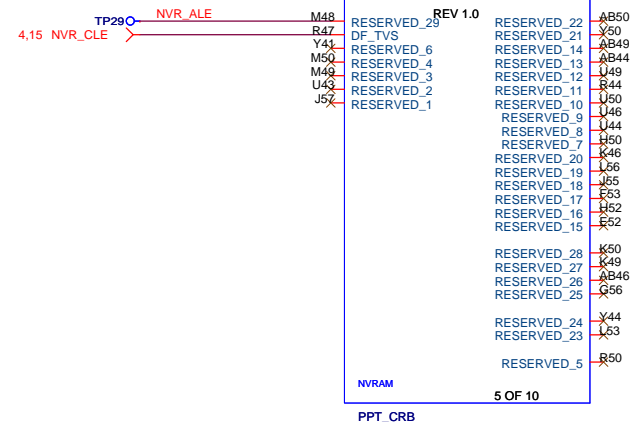
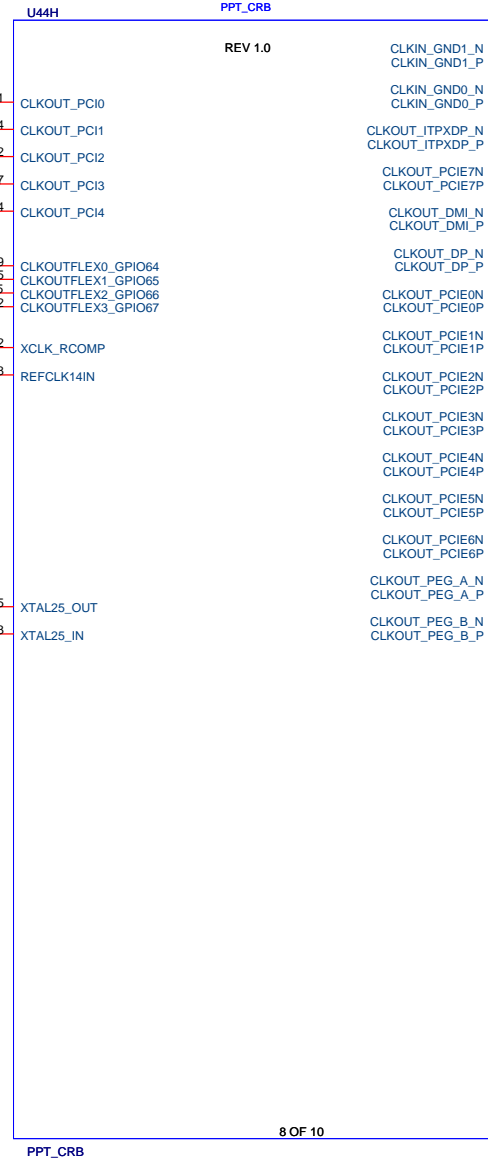
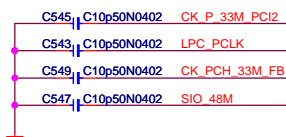
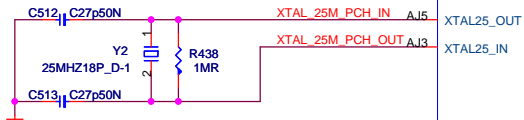
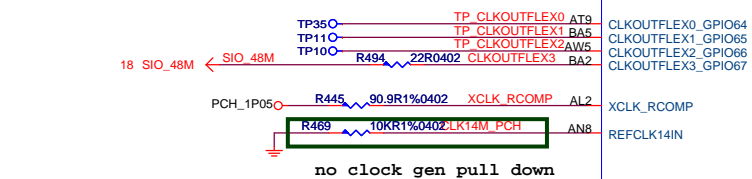


OB1-7733003

LPC Debug Port

TO SIO

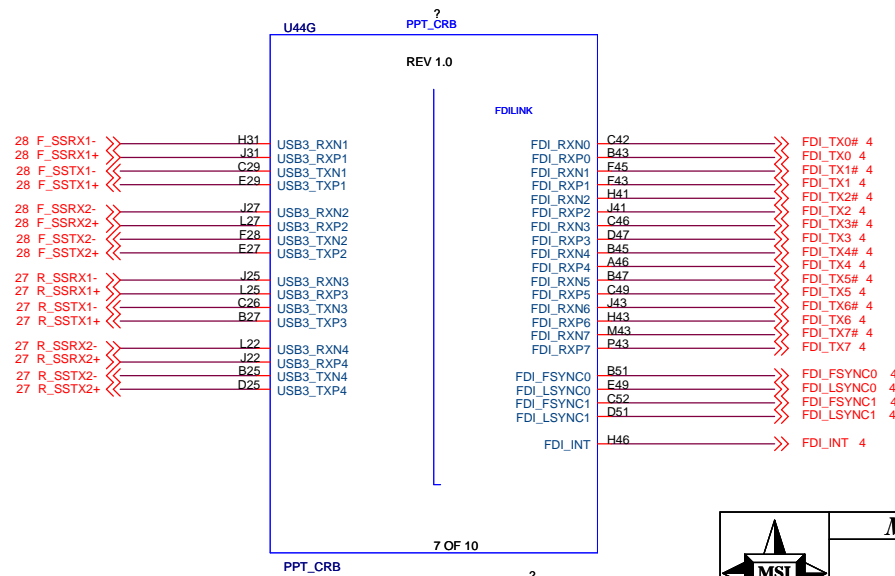
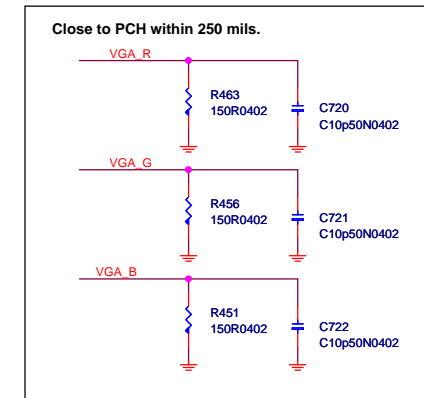
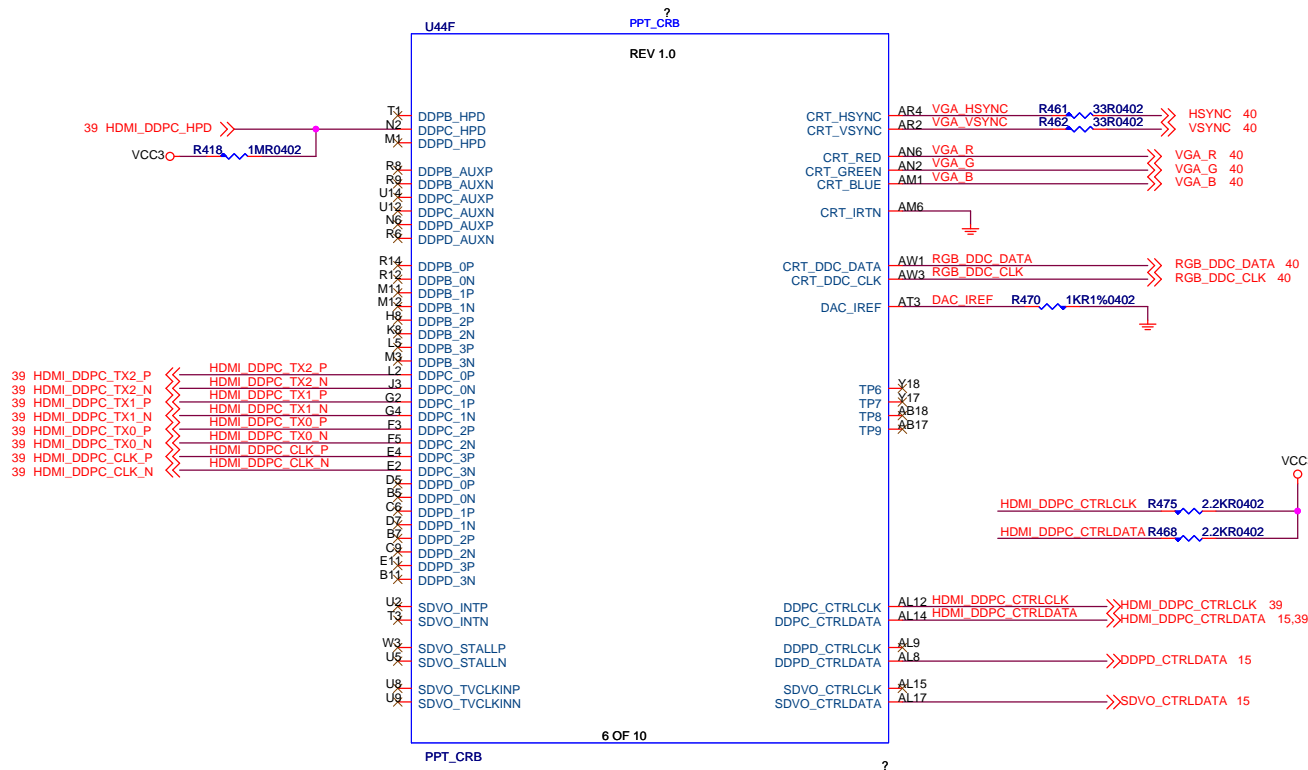
PCICLK LOOPBACK



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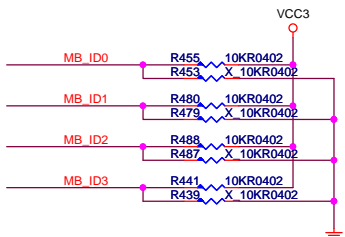
Size	Document Description	Rev
	Panther Point - CLK	11
Date:	Tuesday, March 13, 2012	Sheet 11 of 45



## Gen3

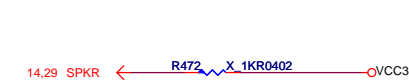


Size	Document Description <b>Panther Point - SATA</b>	Rev <b>11</b>
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REQUIRED STRAPS

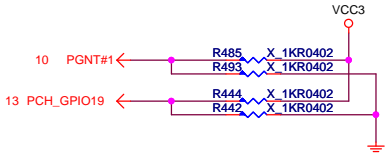


The signal has a weak internal pull-down.  
If the signal is sampled high, this indicates that the system is strapped to the "No Reboot" mode."  
(PCH will disable the TCO Timer system reboot feature).



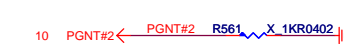
1: INIT3\_3V to asserted for 16 PCI clock  
to reset the processor by some events occur.  
0: Can not to reset the processor.

This signal has a weak internal pull-up.  
INIT3\_3# do not Pull low

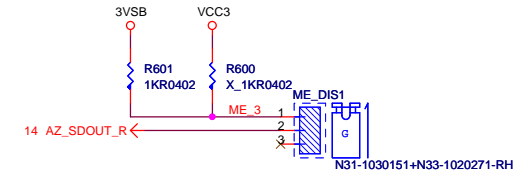


Balls have an internal weak pull-up - Default destination is SPI

BOOT DEVICE	GNT1#/GPIO51	SATA1GP/GPIO19
SPI (Default )	floating	floating
PCI	0	floating
LPC	0	0



ESI Strap  
(Server/Workstation Only)  
This Signal has a weak internal pull-up  
Do not pull low.  
Tying this strap low configures DMI for ESI compatible  
operation.

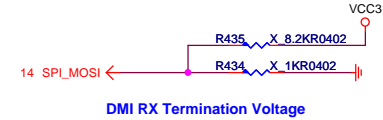


N41-1030141-H06

Disable ME in Manufacturing mode

2 - 3	Normal
1 - 2	Disable ME

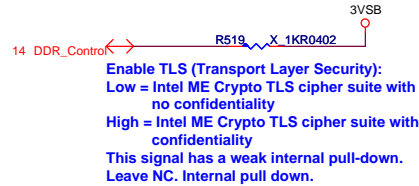
Flash Descriptor Security Override / IntelME Debug mode  
HDA\_SDO need to be pulled high to disable flash security and ME  
Signal has a weak internal pull-down.



DMI RX Termination Voltage



DMI and FDI Tx/Rx Termination Voltage  
Internal weak pull Down. Do not pull up.



Enable TLS (Transport Layer Security):  
Low = Intel ME Crypto TLS cipher suite with  
no confidentiality  
High = Intel ME Crypto TLS cipher suite with  
confidentiality  
This signal has a weak internal pull-down.  
Leave NC. Internal pull down.

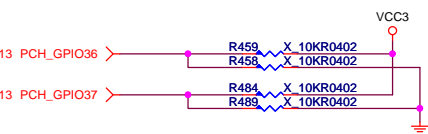


BTM : (Buffer Through Mode)  
Leave floating. Do not pull low.  
FCIM : (Full Clock Integration Mode)  
Pull low with 1k Ohm to ground.

FCIM. Can be override by softstrap through ME.  
This signal has a weak internal pull-up.



The On-Die PLL voltage regulator  
(Default) Enabled when sampled high  
Disabled when sampled low  
Internal weak pull up. Do not pull low.



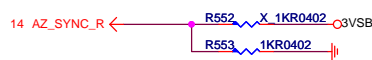
Since Pin has internal pull-down  
following guidelines are required to be

- A) When Used as SATA2GP/SATA3GP  
use 10K external pull-up that is enabled
- B) When Used as GP Input (Pin HW default) –  
Ensure GPI is not driven high during strap

When Unused as GPIO or SATA[x]GP – Use 8.2K-  
10K pull-down to ground.



The signal has a weak internal pull-up.  
If the signal is sampled low, this indicates that the system  
is strapped to the "topblock swap" mode  
(PCH inverts A16 for all cycles targeting BIOS space).



On-Die PLL Voltage Regulator Voltage Select

Internal weak pull down. Do not pull up.  
High: VccVRM by 1.5 V  
Low : VccVRM by 1.8 V

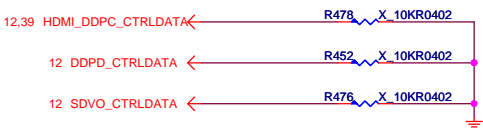


Integrated 1.05V VRM Enable / Disable  
When high :Integrated 1.05 V VRMs is enabled  
when low :External VR power source is used for DcpSus

NOTE: External VR powering option is for Mobile Only.  
Other systems should not pull the strap low.



Deep S4/S5 Well On-Die Voltage Regulator Enable  
If strap is sampled high, the Integrated Deep S4/S5 Well  
(DSW) On-Die VR mode is enabled.



This signal has a weak internal pull-down.  
When '1'- Port B/C/D is detected;  
When '0'- Port B/C/D is not detected

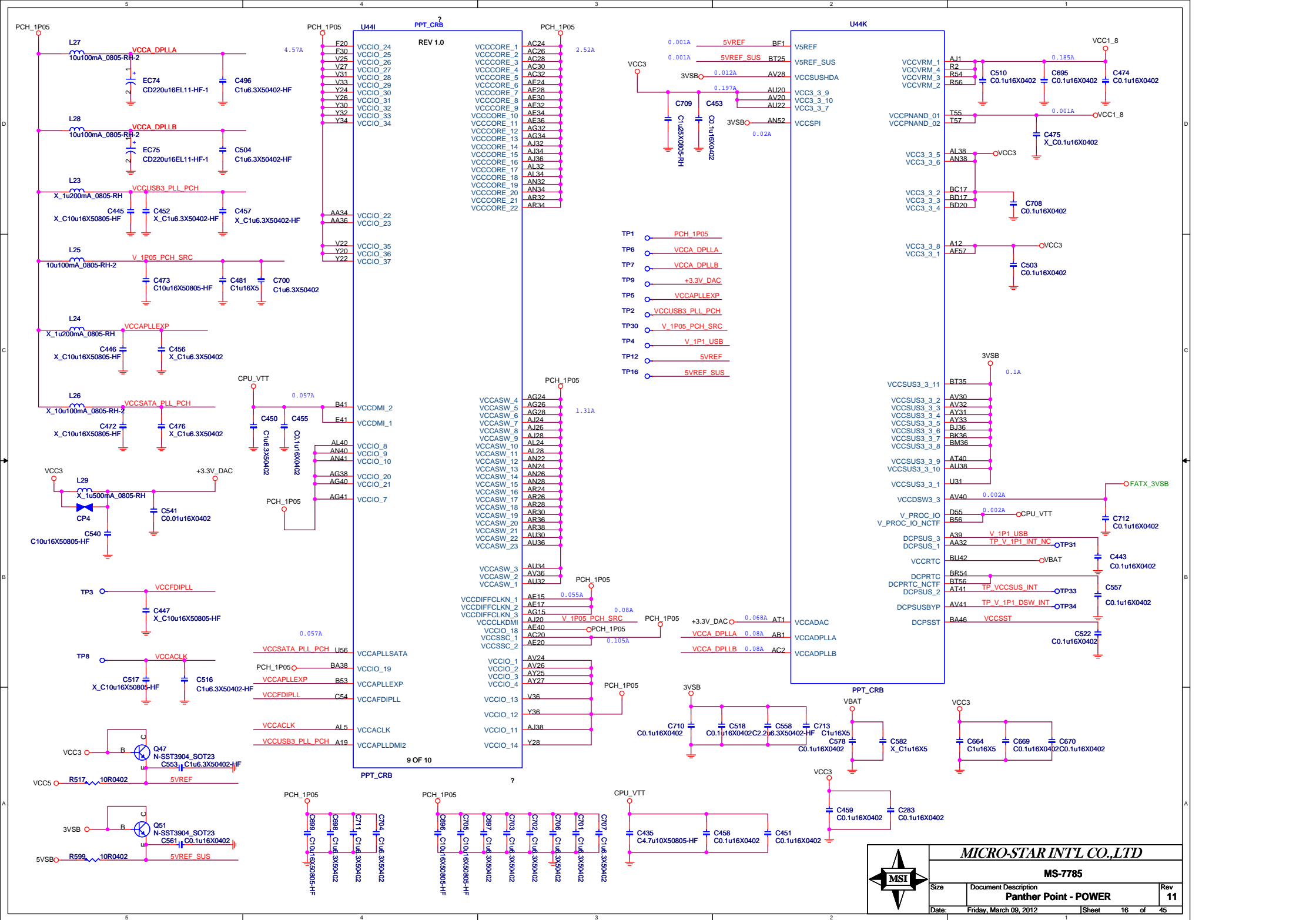


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	Panther Point - STRAP	11
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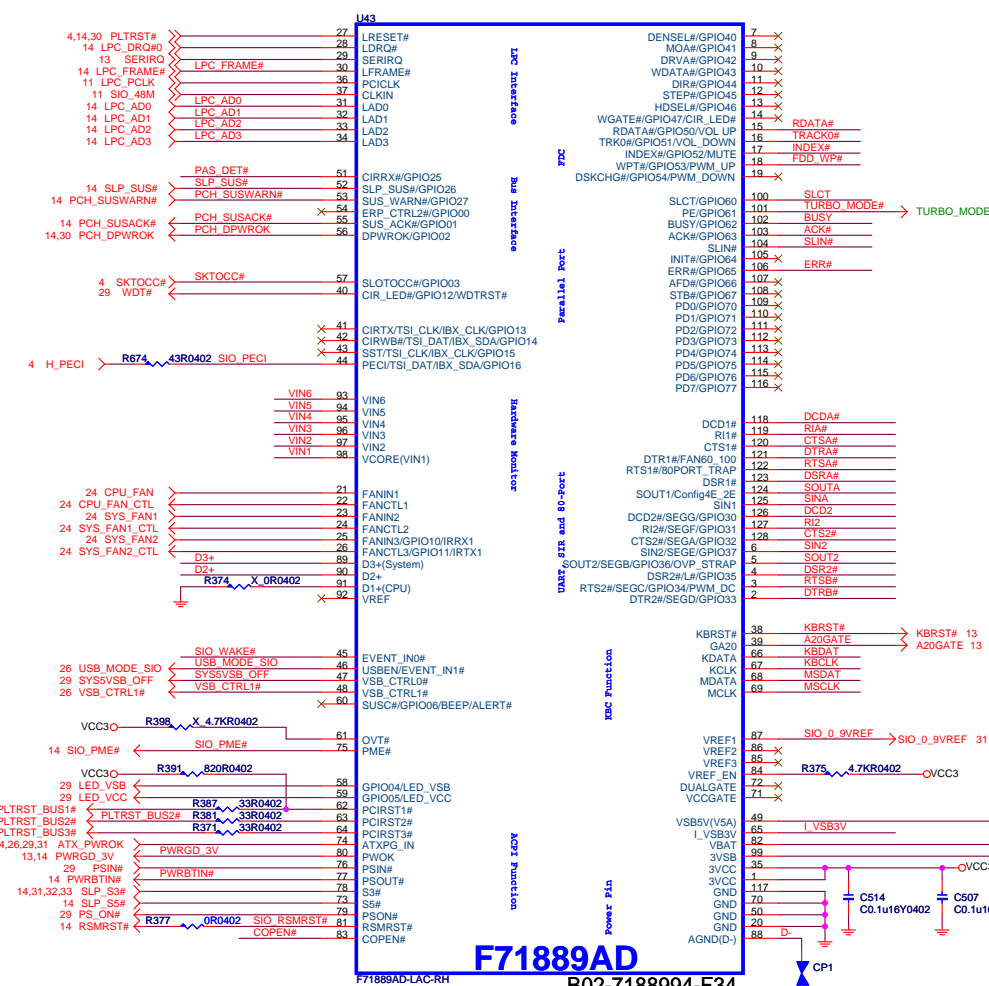


PPT\_CR8

BC15	VSS_125	VSS_5	A26
BC20	VSS_126	VSS_6	A29
BC27	VSS_127	VSS_7	A42
BC31	VSS_128	VSS_8	A49
BC36	VSS_129	VSS_9	A9
BC38	VSS_130	VSS_10	AA20
BC47	VSS_131	VSS_11	AA22
BC51	VSS_132	VSS_12	AA24
BD25	VSS_133	VSS_13	AA28
BD33	VSS_134	VSS_14	AA30
BE12	VSS_135	VSS_15	AA38
BE20	VSS_136	VSS_16	AA38
BE25	VSS_137	VSS_17	AB11
BE33	VSS_138	VSS_18	AB15
BE34	VSS_139	VSS_19	AB16
BE46	VSS_140	VSS_20	AB41
BE52	VSS_141	VSS_21	AB47
BE6	VSS_142	VSS_22	AB52
BG22	VSS_143	VSS_23	AB57
BG27	VSS_144	VSS_24	AB57
BG31	VSS_145	VSS_25	AC22
BG33	VSS_146	VSS_26	AC34
BG38	VSS_147	VSS_27	AC38
BG38	VSS_148	VSS_28	AC38
BG42	VSS_149	VSS_29	AC38
BU1	VSS_150	VSS_30	AC4
BU15	VSS_151	VSS_31	AC54
BU15	VSS_152	VSS_32	AE18
BU15	VSS_153	VSS_33	AE22
BK20	VSS_154	VSS_34	AE26
BK41	VSS_155	VSS_35	AE38
BK52	VSS_156	VSS_36	AE38
BK6	VSS_157	VSS_37	AE4
BM1	VSS_158	VSS_38	AE47
BM12	VSS_159	VSS_39	AE9
BM16	VSS_160	VSS_40	AE52
BM22	VSS_161	VSS_41	AE6
BM23	VSS_162	VSS_42	AG11
BM28	VSS_163	VSS_43	AG14
BM32	VSS_164	VSS_44	AG14
BM40	VSS_165	VSS_45	AG22
BM42	VSS_166	VSS_46	AG30
BM48	VSS_167	VSS_47	AG38
BM5	VSS_168	VSS_48	AG43
BM5	VSS_169	VSS_49	AG44
BM6	VSS_170	VSS_50	AG44
BM6	VSS_171	VSS_51	AG46
BP3	VSS_172	VSS_52	AG50
BP3	VSS_173	VSS_53	AG53
BP35	VSS_174	VSS_54	AG52
BP35	VSS_175	VSS_55	AH52
BP35	VSS_176	VSS_56	AH6
BP35	VSS_177	VSS_57	AJ22
BP35	VSS_178	VSS_58	AJ30
BP35	VSS_179	VSS_59	AJ32
BP35	VSS_180	VSS_60	AK6
BP35	VSS_181	VSS_61	AK6
BP35	VSS_182	VSS_62	AL11
BP35	VSS_183	VSS_63	AL18
BP35	VSS_184	VSS_64	AL20
BP35	VSS_185	VSS_65	AL26
BP35	VSS_186	VSS_66	AL30
BP35	VSS_187	VSS_67	AL36
BP35	VSS_188	VSS_68	AL41
BP35	VSS_189	VSS_69	AL46
BP35	VSS_190	VSS_70	AL46
BP35	VSS_191	VSS_71	AL47
BP35	VSS_192	VSS_72	AM52
BP35	VSS_193	VSS_73	AM57
BP35	VSS_194	VSS_74	AN11
BP35	VSS_195	VSS_75	AN11
BP35	VSS_196	VSS_76	AN12
BP35	VSS_197	VSS_77	AN15
BP35	VSS_198	VSS_78	AN17
BP35	VSS_199	VSS_79	AN18
BP35	VSS_200	VSS_80	AN20
BP35	VSS_201	VSS_81	AN20
BP35	VSS_202	VSS_82	AN38
BP35	VSS_203	VSS_83	AN4
BP35	VSS_204	VSS_84	AN43
BP35	VSS_205	VSS_85	AN47
BP35	VSS_206	VSS_86	AN4
BP35	VSS_207	VSS_87	AN9
BP35	VSS_208	VSS_88	AR20
BP35	VSS_209	VSS_89	AR22
BP35	VSS_210	VSS_90	AR52
BP35	VSS_211	VSS_91	AR6
BP35	VSS_212	VSS_92	AT18
BP35	VSS_213	VSS_93	AT18
BP35	VSS_214	VSS_94	AT18
BP35	VSS_215	VSS_95	AT17
BP35	VSS_216	VSS_96	AT52
BP35	VSS_217	VSS_97	AT6
BP35	VSS_218	VSS_98	AT6
BP35	VSS_219	VSS_99	AT6
BP35	VSS_220	VSS_100	AU24
BP35	VSS_221	VSS_101	AU28
BP35	VSS_222	VSS_102	AU28
BP35	VSS_223	VSS_103	AU5
BP35	VSS_224	VSS_104	AV12
BP35	VSS_225	VSS_105	AV12
BP35	VSS_226	VSS_106	BA49
BP35	VSS_227	VSS_107	BA49
BP35	VSS_228	VSS_108	BB52
BP35	VSS_229	VSS_109	BB52
BP35	VSS_230	VSS_110	BB52
BP35	VSS_231	VSS_111	BB52
BP35	VSS_232	VSS_112	BB52
BP35	VSS_233	VSS_113	BB52
BP35	VSS_234	VSS_114	BB52
BP35	VSS_235	VSS_115	BB52
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BP35	VSS_239	VSS_119	BB52
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BP35	VSS_244	VSS_124	BB52
BP35	VSS_245	VSS_125	BB52
BP35	VSS_246	VSS_126	BB52
BP35	VSS_247	VSS_127	BB52
BP35	VSS_248	VSS_128	BB52
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BP35	VSS_250	VSS_130	BB52
BP35	VSS_251	VSS_131	BB52
BP35	VSS_252	VSS_132	BB52
BP35	VSS_253	VSS_133	BB52
BP35	VSS_254	VSS_134	BB52
BP35	VSS_255	VSS_135	BB52
BP35	VSS_256	VSS_136	BB52
BP35	VSS_257	VSS_137	BB52
BP35	VSS_258	VSS_138	BB52
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BP35	VSS_260	VSS_140	BB52
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BP35	VSS_262	VSS_142	BB52
BP35	VSS_263	VSS_143	BB52
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BP35	VSS_274	VSS_154	BB52
BP35	VSS_275	VSS_155	BB52
BP35	VSS_276	VSS_156	BB52
BP35	VSS_277	VSS_157	BB52
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BP35	VSS_282	VSS_162	BB52
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BP35	VSS_284	VSS_164	BB52
BP35	VSS_285	VSS_165	BB52
BP35	VSS_286	VSS_166	BB52
BP35	VSS_287	VSS_167	BB52
BP35	VSS_288	VSS_168	BB52
BP35	VSS_289	VSS_169	BB52
BP35	VSS_290	VSS_170	BB52

U44J  
PPT\_CR8  
REV 1.0  
?  
?  
10 OF 10

VSS_231	L12
VSS_232	L17
VSS_233	L38
VSS_234	L41
VSS_235	L43
VSS_236	M20
VSS_237	M22
VSS_238	M25
VSS_239	M27
VSS_240	M31
VSS_241	T52
VSS_242	T6
VSS_243	U11
VSS_244	U17
VSS_245	U22
VSS_246	U27
VSS_247	U33
VSS_248	U38
VSS_249	U41
VSS_250	U47
VSS_251	U53
VSS_252	U57
VSS_253	W5
VSS_254	W1
VSS_255	W55
VSS_256	W57
VSS_257	Y11
VSS_258	Y15
VSS_259	Y43
VSS_260	Y46
VSS_261	Y47
VSS_262	Y48
VSS_263	Y52
VSS_264	Y6
VSS_265	A4
VSS_266	AE1
VSS_267	BM1
VSS_268	BM67
VSS_269	BP1
VSS_270	BP57
VSS_271	BP57
VSS_272	BP57
VSS_273	BP57
VSS_274	BP57
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VSS_491	BP57

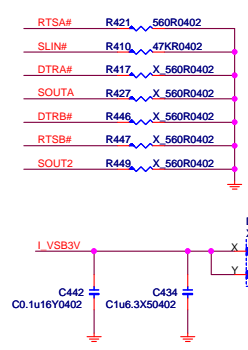


**Power On Strapping Table**  
Default: Internal Pull-up

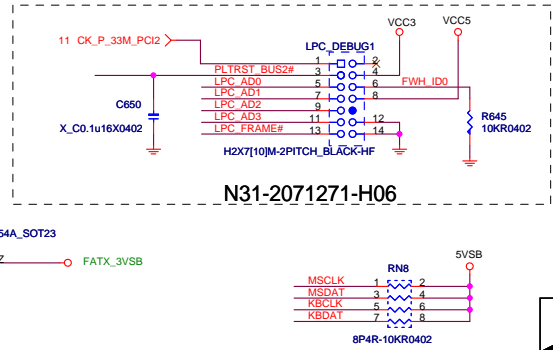
PLTRST_BUS1#	SLOT1 SLOT3
PLTRST_BUS2#	LPC Debug Port eSATA
PLTRST_BUS3#	SLOT2 SLOT4

Symbol	Value	Description
RTSB#	1	Fan control mode: PWM mode.
	0	Fan control mode: DAC mode.
SLIN#	PU-1k	Pin 100-116 as LPT interfaces
	PU-20k	Pin 100-116 as PVID Controller
	PD-1k	Pin 102/103/111/112 as SVID Controller
	PD-47k	Pin 100-103 and pin 105-116 as GPIO pins
DTRA#	1	Fan full duty is 60%.
	0	Fan full duty is 100%.
RTSA#	1	Enable the 80 port function.
	0	Disable the 80 port function.
SOUTA	1	Configuration Register I/O port is 4E/4F.
	0	Configuration Register I/O port is 2E/2F.
SOUT2	1	OVP warning mode
	0	OVP force mode

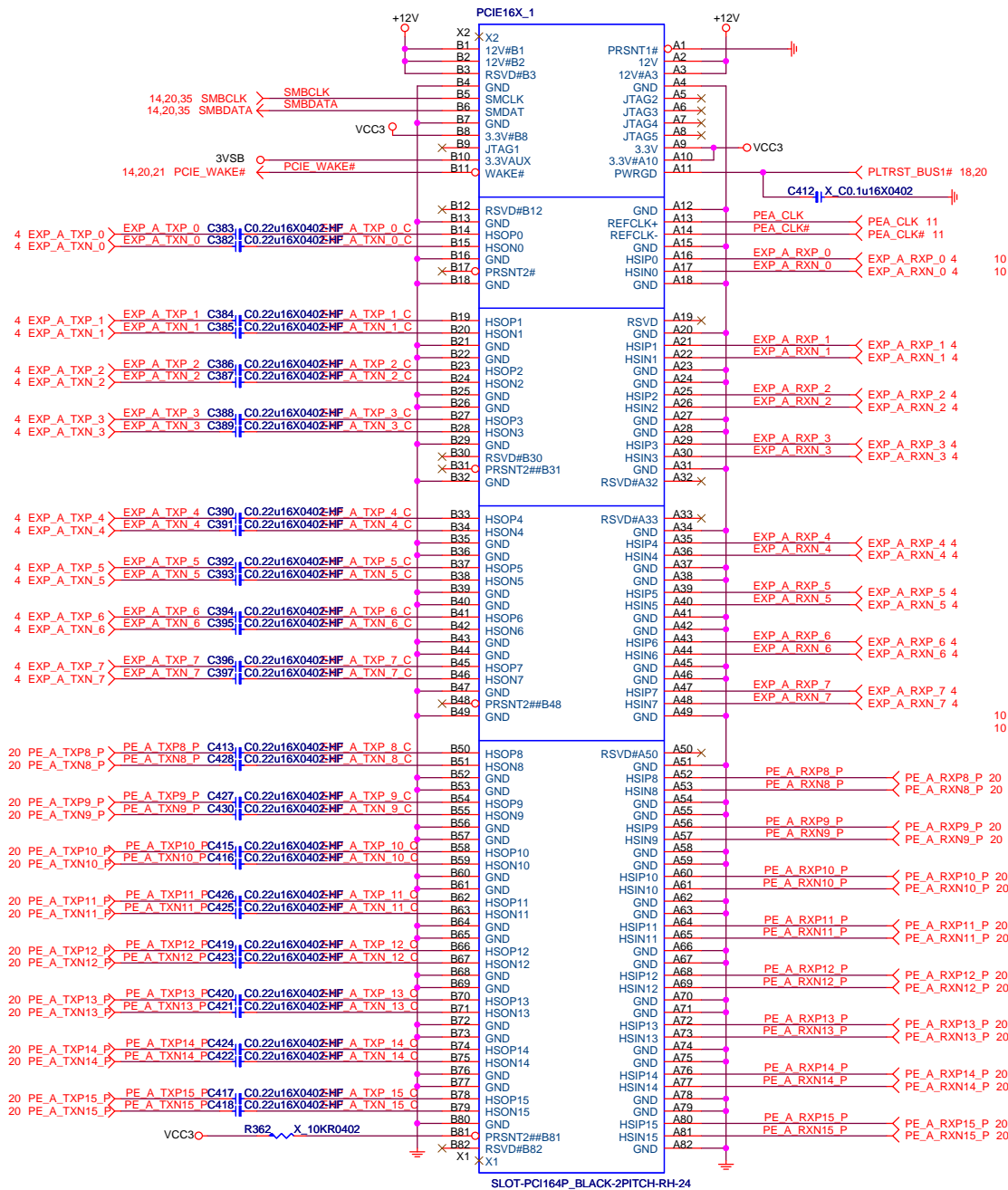
**Power on Strapping Option**



**LPC Debug Port**

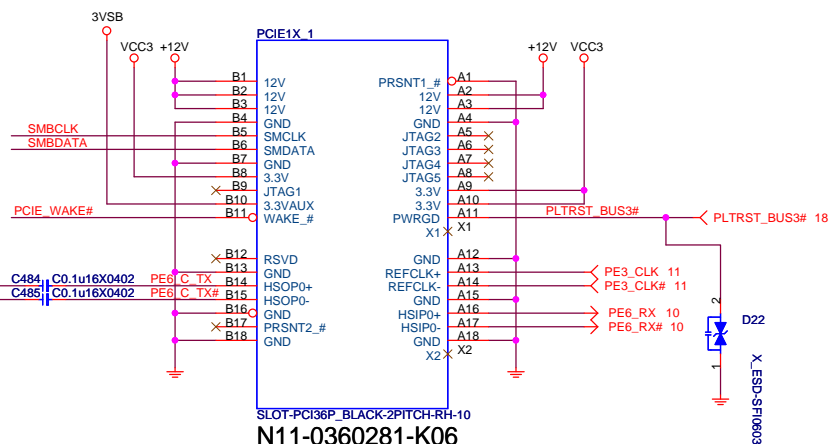


# PCI EXPRESS X16 SLOT

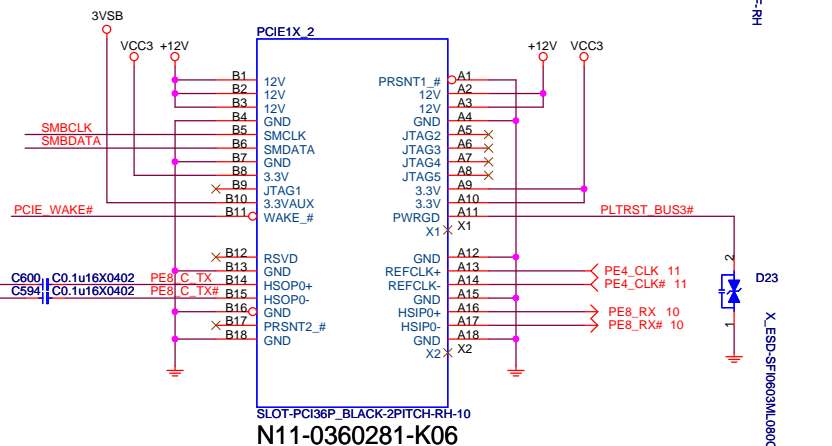


N11-1640851-W02

# PCI EXPRESS x1-PORT



# PCI EXPRESS x1-PORT



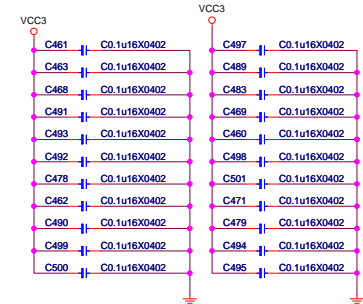
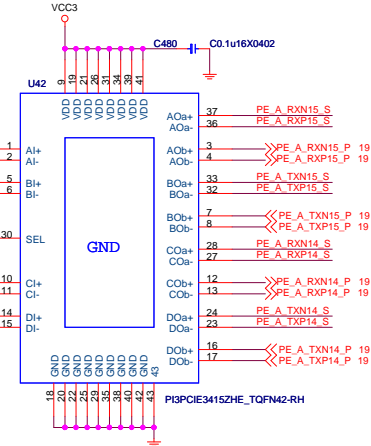
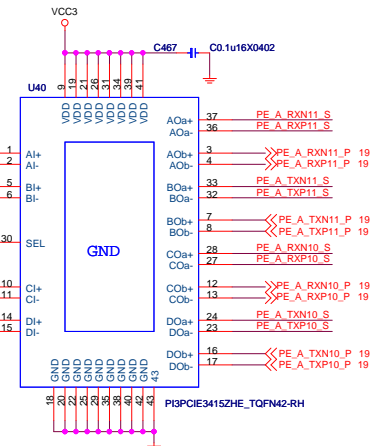
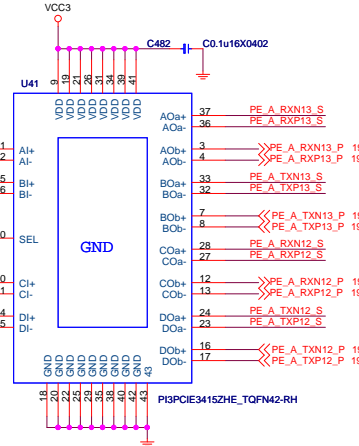
N11-0360281-K06



MICRO-STAR INTL CO.,LTD

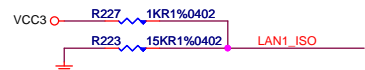
MS-7785

Size	Document Description	Rev
	PCIE x16 & x1	11
Date:	Wednesday, March 14, 2012	Sheet 19 of 45

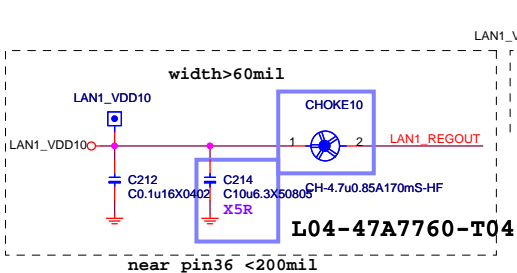
[illegible]

Size	Document Description	Rev
	<b>PCIE X8</b>	<b>11</b>
Date:	Wednesday, March 14, 2012	Sheet 20 of 45

# RTL8111E Giga LAN

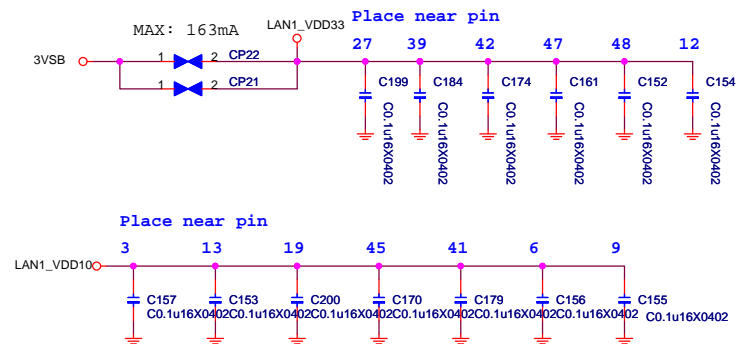


```
1: Enable switching regulator
0: Disable switching regulator
```



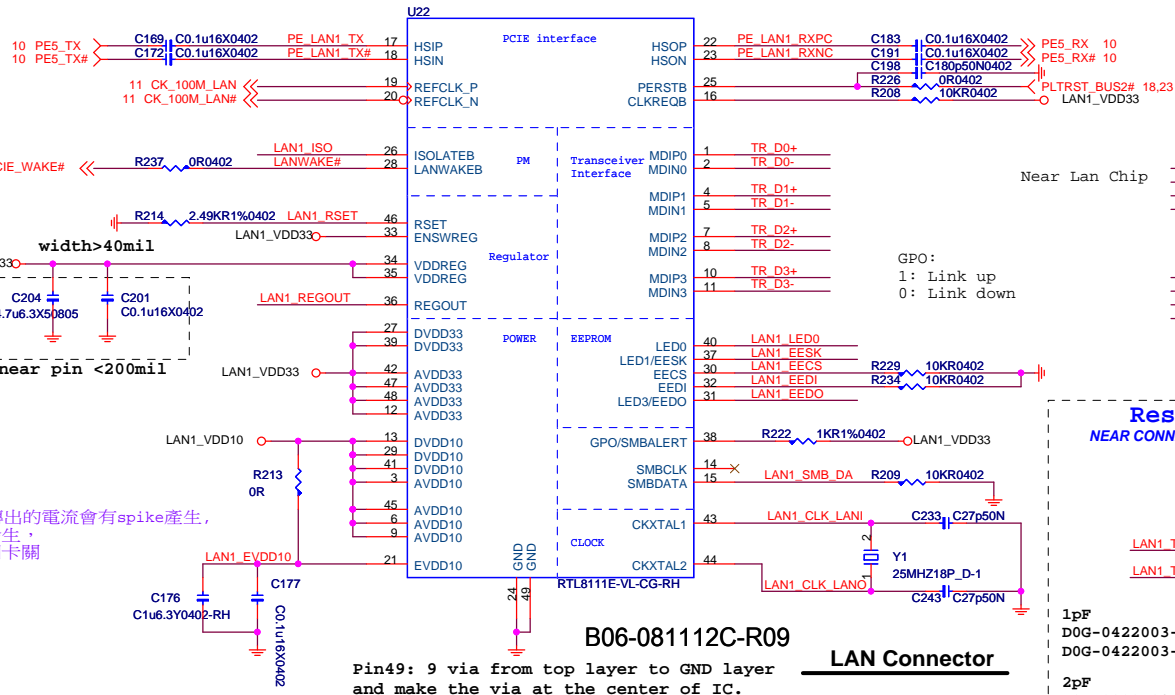
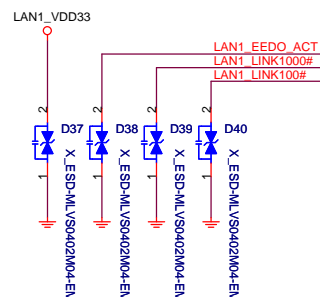
2.2uH在PFM/PWM mode 切換的時候, switching regulator 轉出的電流會有spike產生, 評估日後會有issue風險, 而4.7uH則沒有此抽大電流情況發生, 更進一步為了降低日後的debug effort, 在此必須要先做個卡關 為了避免1.05V轉出電壓會有不正常的情況發生, 也許是ripple過大或者電壓偏高低等風險存在, 因此這類產品才會強調要限制料件種類

3.3v Power on rise time : 1~100ms.

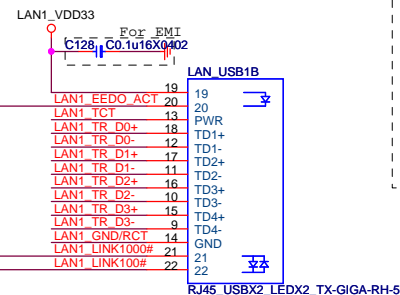


## 8111E POWER Consumption

	3.3V	mW
10 M Idle/TxRx	12/66	40/218
100 M Idle/TxRx	31/44	102/145
Giga Idle/TxRx	135/163	452/538
ALDPS	4	13



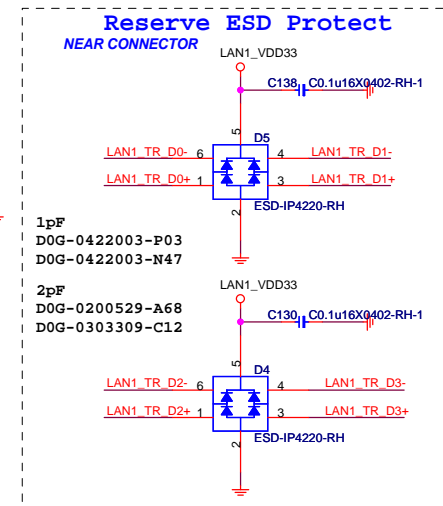
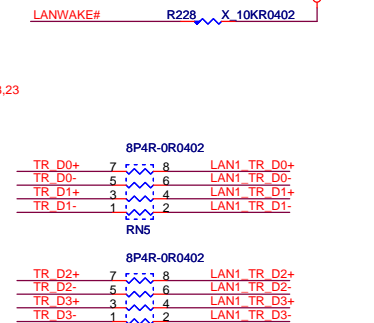
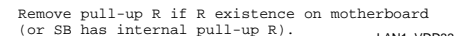
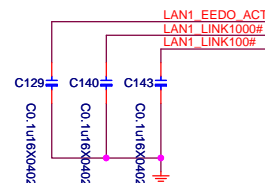
Pin49: 9 via from top layer to GND layer  
and make the via at the center of IC.







N58-22F0731-F02

R14, R15, R17請依據所使用的LAN connector上的LED亮度去調整阻值

only support LED0+LED1/LED1+LED3 dual color LED combinations when using EEPROM



Giga-Lan		10/100-Lan	
N58-22F0731-F02		N58-22F0061-S4	
N58-22F0731-S42		N58-22F0061-F0	
N58-22F0731-I60			
Link	Yellow	Link	Yellow
Active	Blinking	Active	Blinking
1000	Orange	100	Green
100	Green	10	None
10	None		
19		19	
20	Yellow	20	Yellow
21		21	
22	Green	22	Green



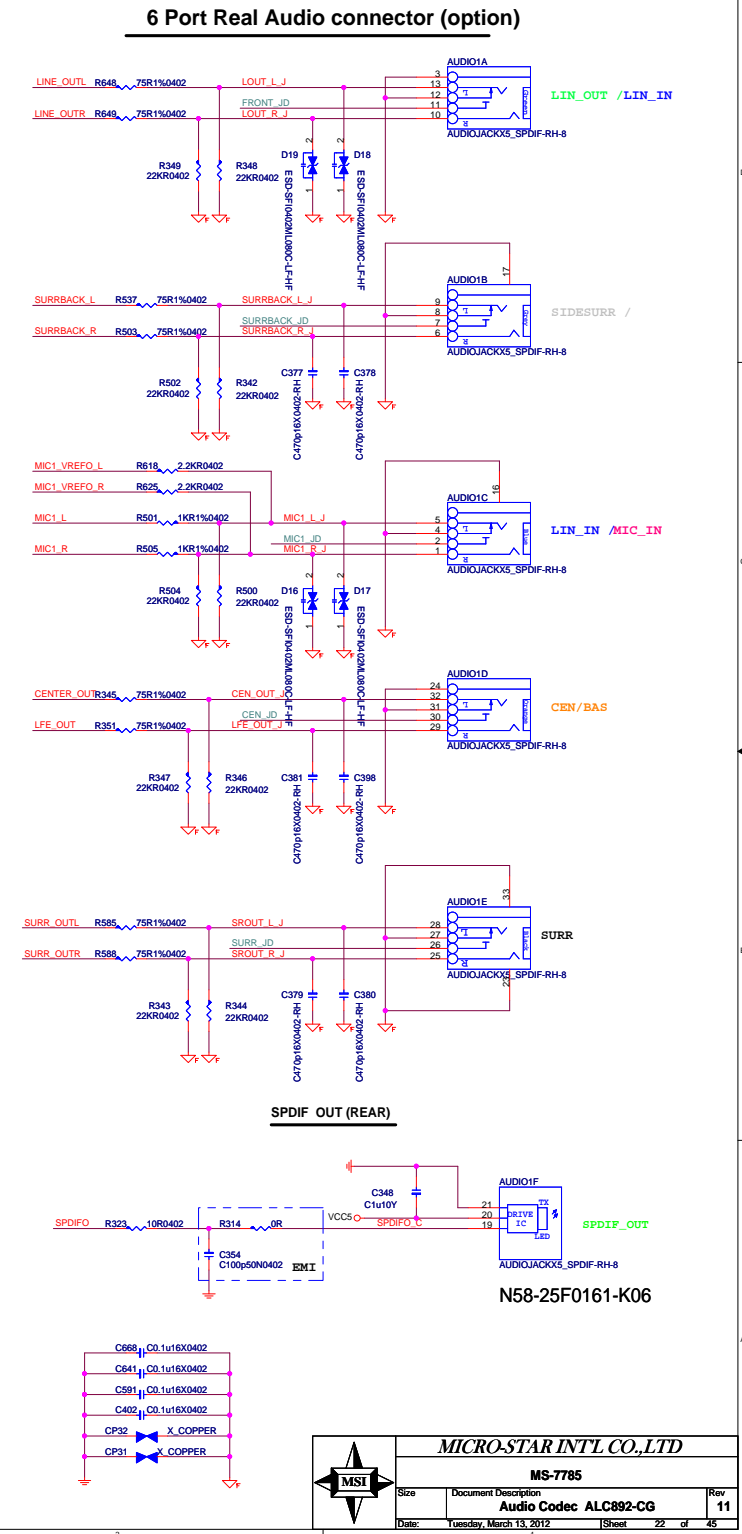
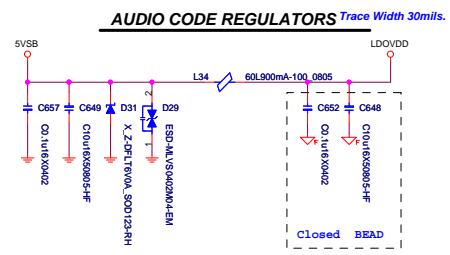
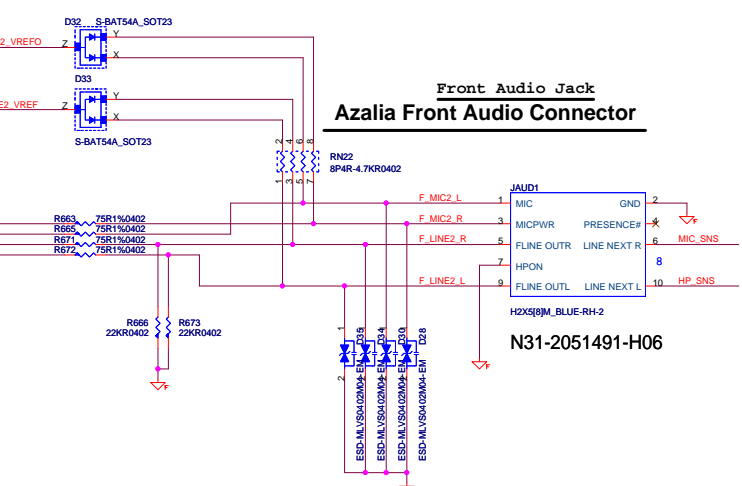
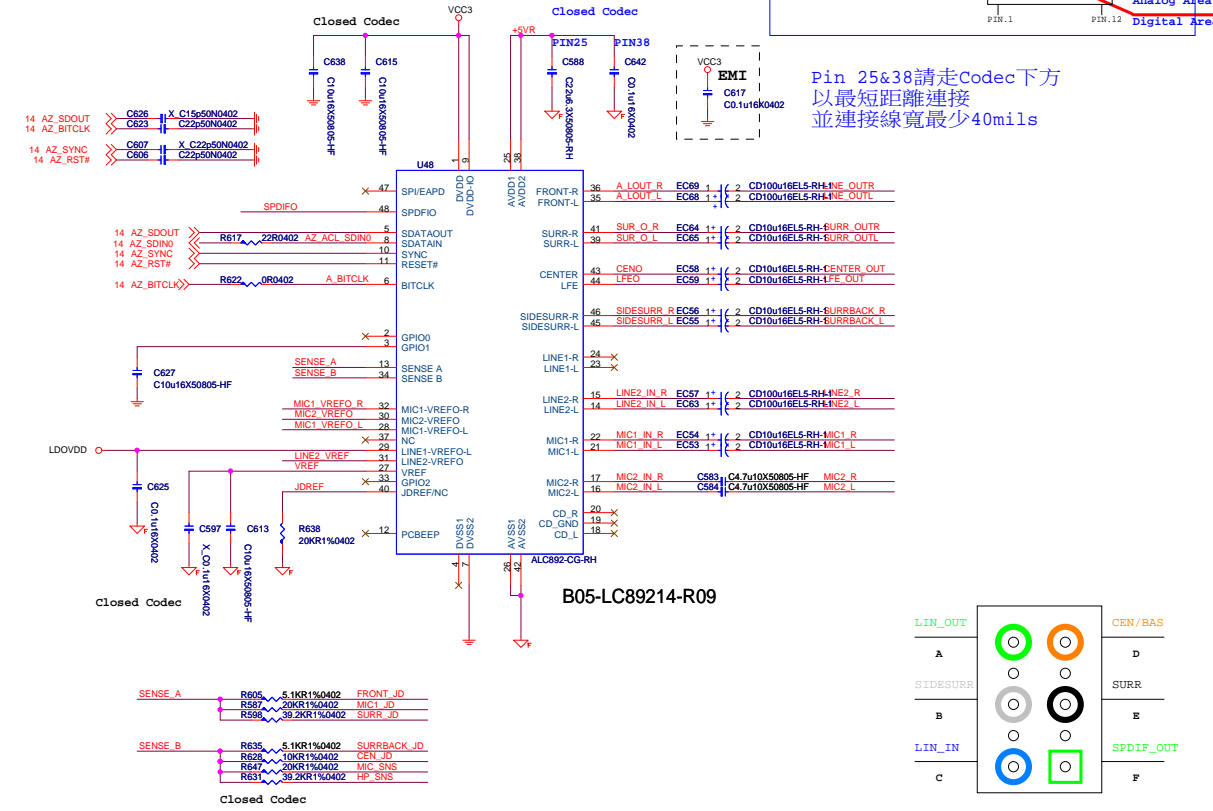
***MICRO-STAR INTL CO.,LTD***

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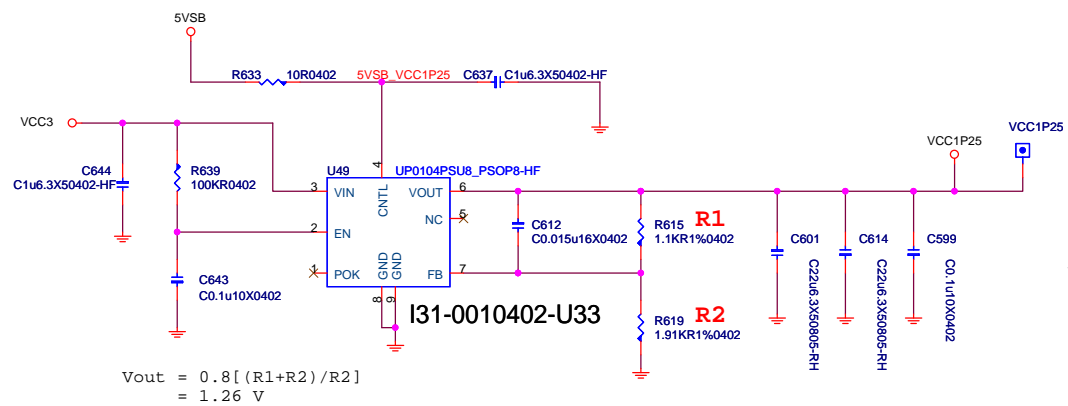
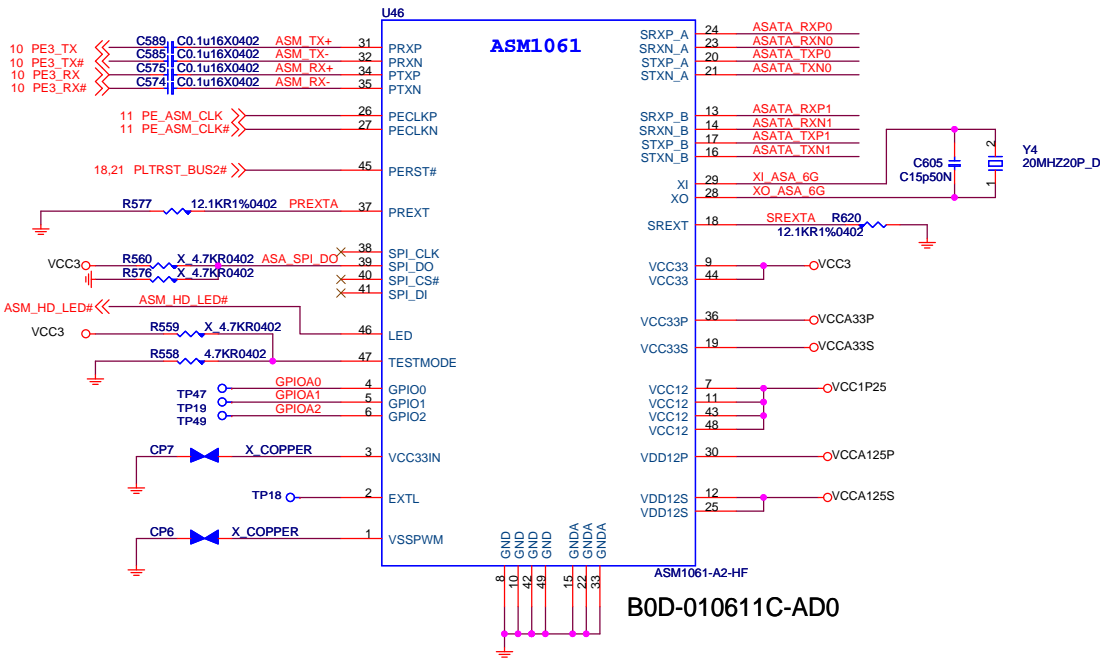
Size	Document Description <b>LAN - RTL8111E-VL-CG</b>	Rev <b>11</b>
Date:	Tuesday, March 13, 2012	Sheet 21 of 45



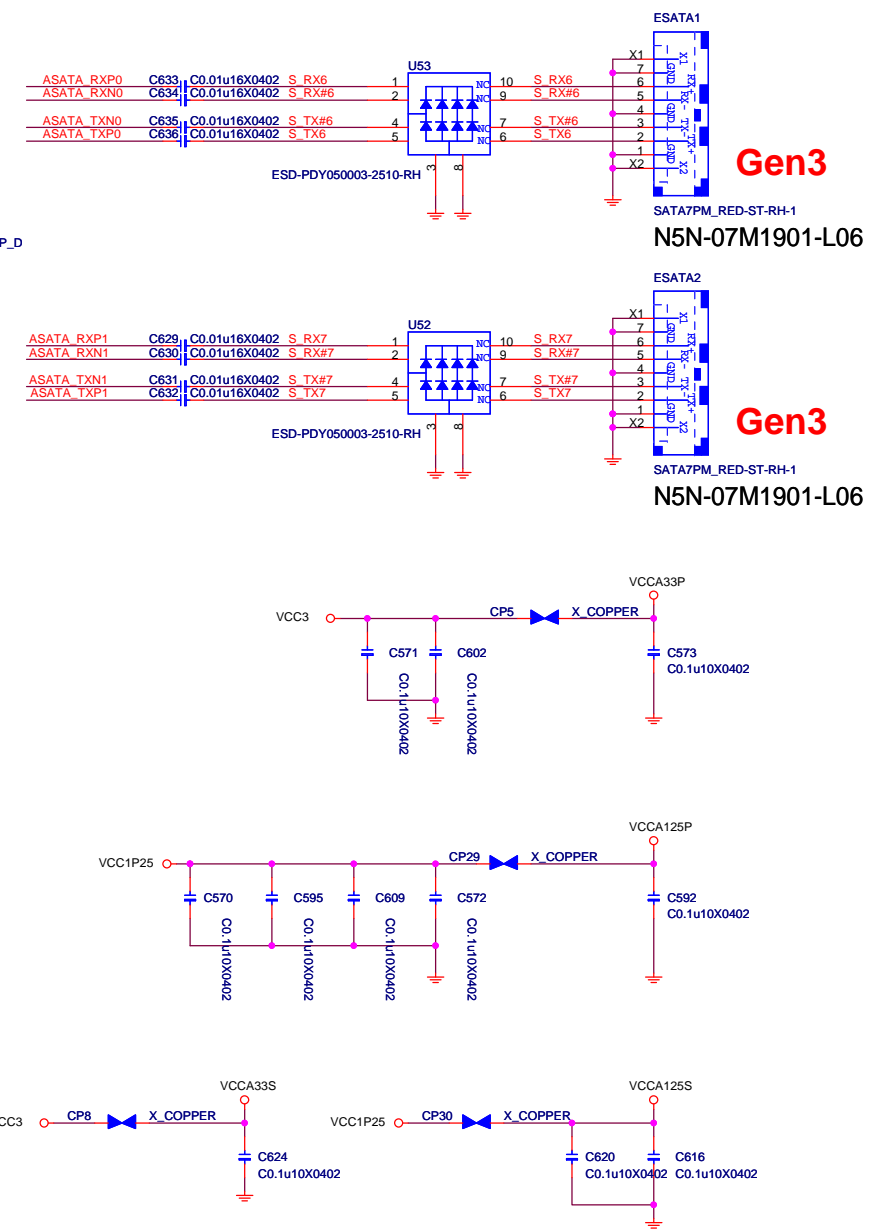
# Azalia Codec - ALC892

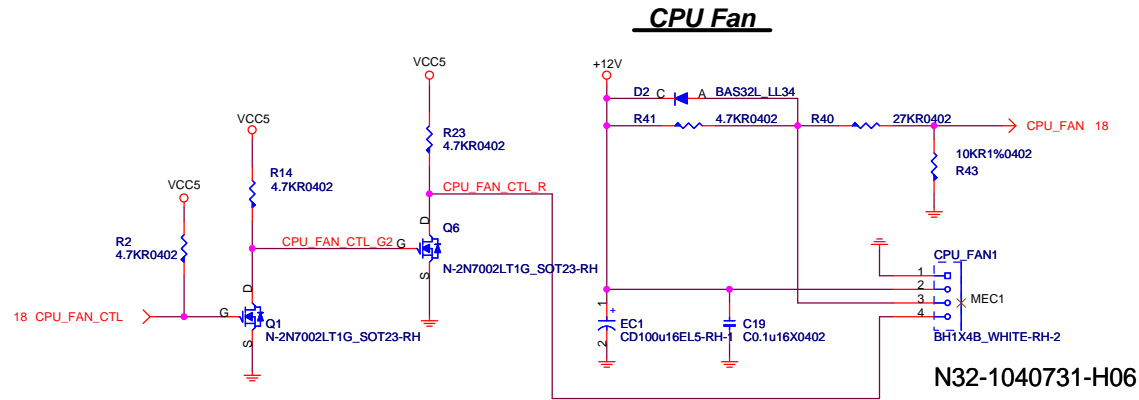




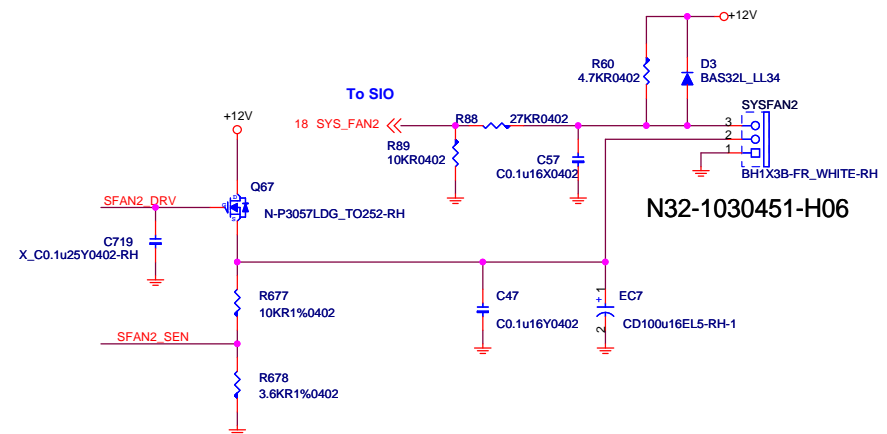
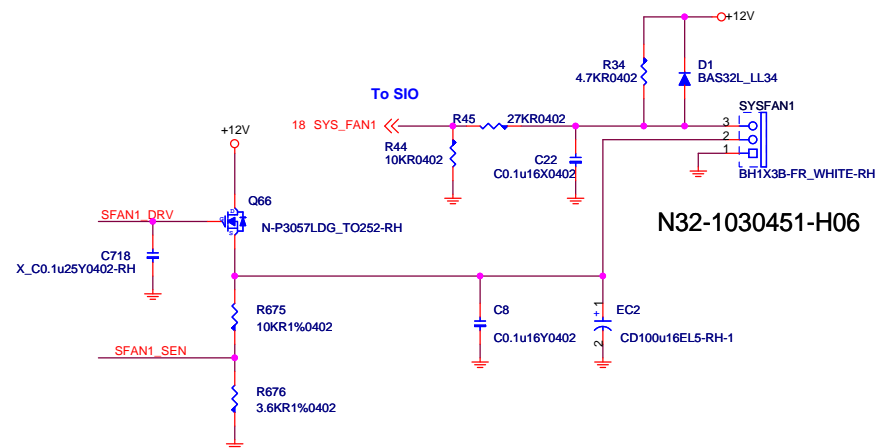
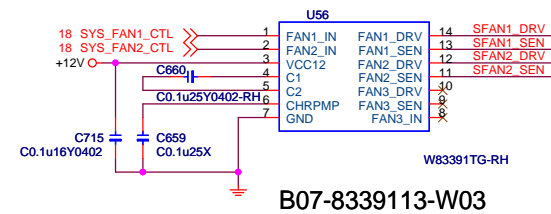


## ESATA Connector





**System Fan 1 , 2**



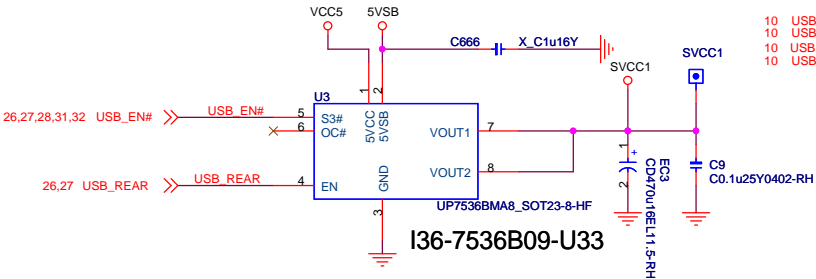
**MICRO-STAR INT'L CO.,LTD**

**MS-7785**

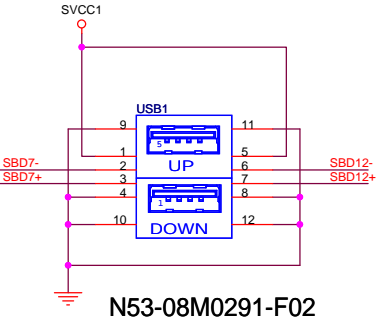
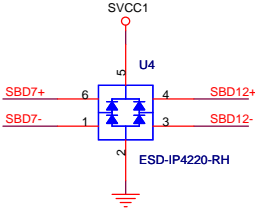
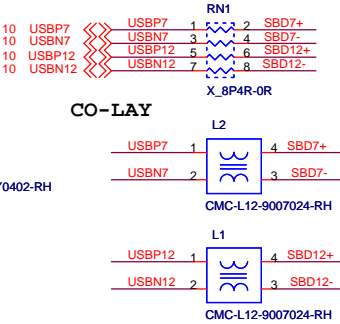
Size	Document Description	Rev
	<b>FAN</b>	<b>11</b>
Date:	Wednesday, March 14, 2012	Sheet 24 of 45

REAR USB PORT

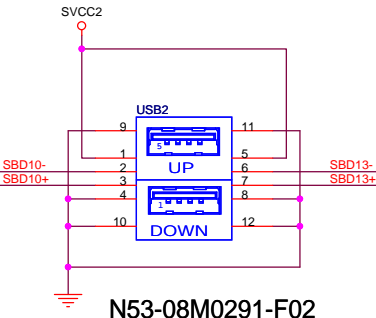
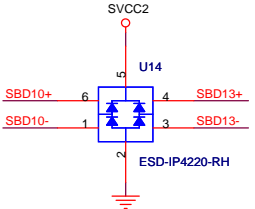
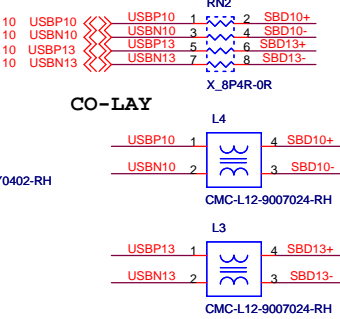
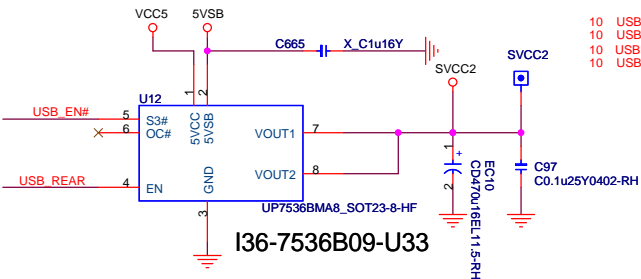
Power Circuit For USB Port 1, 9 ( Connector ?) And KB/MS



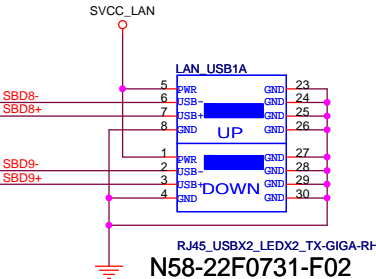
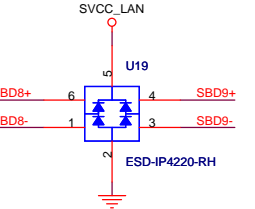
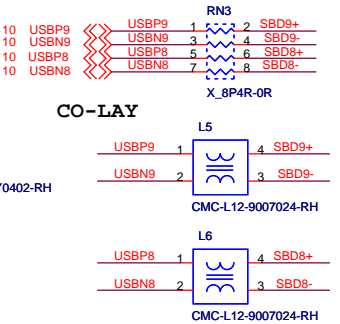
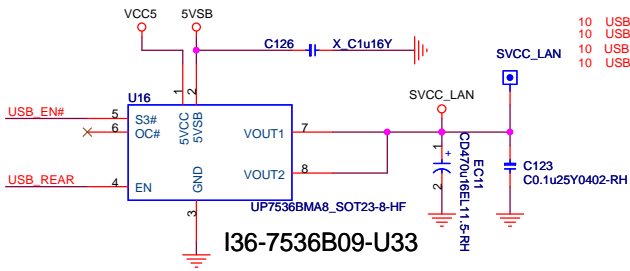
REAR PANEL USB CONNECTOR FOR USB PORT 0,1



Power Circuit For USB Port 1, 9 ( Connector ?) And KB/MS



Power Circuit For USB Port 5, 4 ( Connector ?)



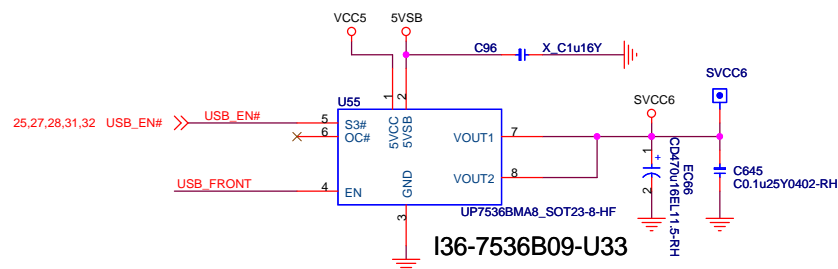
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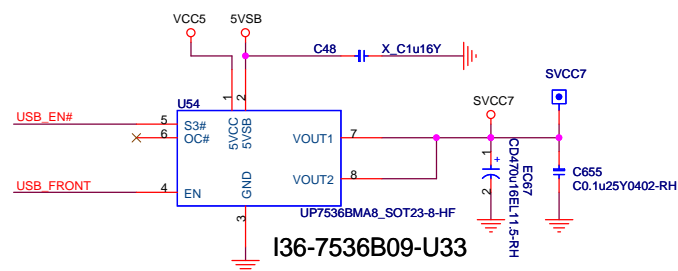
MICRO-STAR INTL CO.,LTD			
MS-7785			
Size	Document Description	Rev	
	Rear USB Connectors	11	
Date:	Tuesday, March 13, 2012	Sheet	25 of 45

## FRONT USB PORT

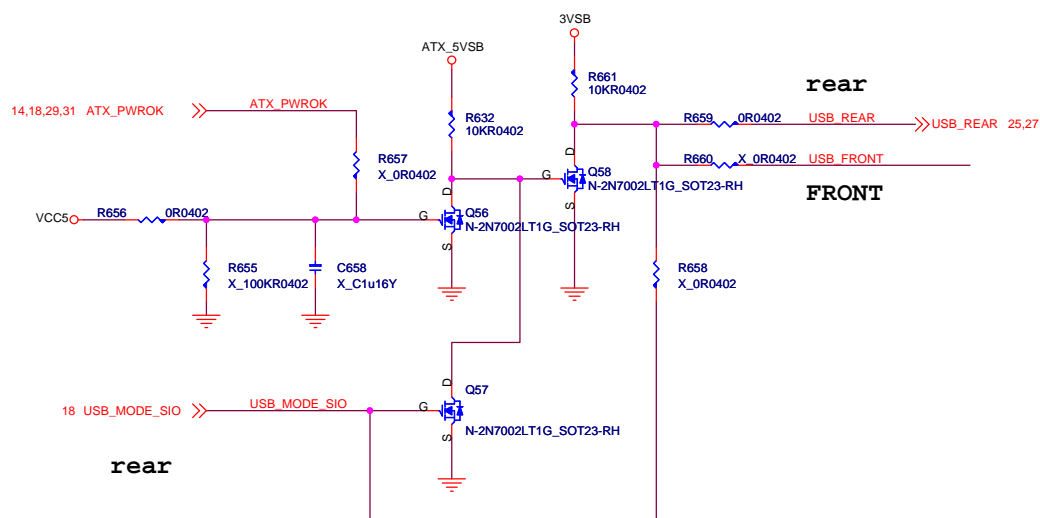
### Power Circuit For USB Port 13, 12



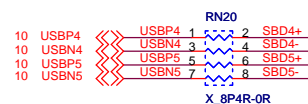
### Power Circuit For USB Port 6 , 7



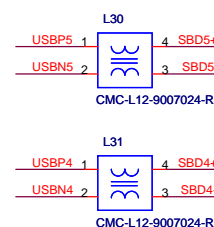
## USB Power Control



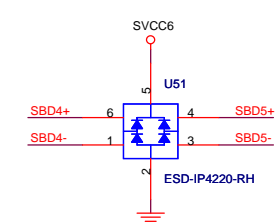
### FRONT PANEL USB CONNECTOR FOR USB PORT 12,13



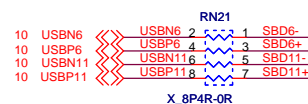
## CO-LAY



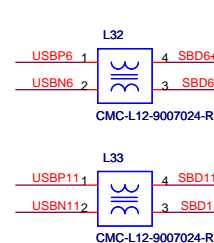
**NEAR USB CONNECTOR**



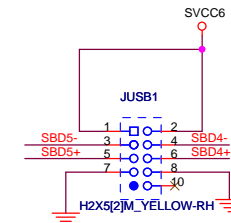
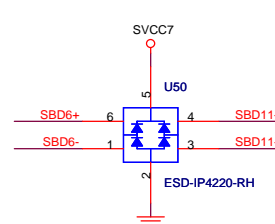
### FRONT PANEL USB CONNECTOR FOR USB PORT 6,7



## CO-LAY

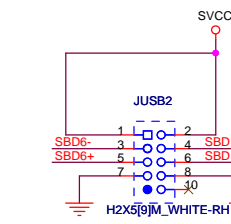


**NEAR USB CONNECTOR**



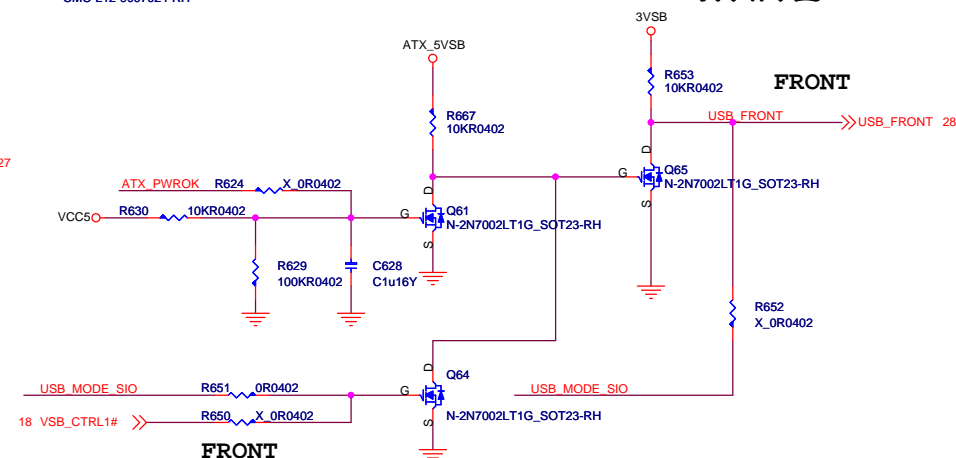
N31-2051321-H06

# YELLOW



N31-2051461-H06

WHITE

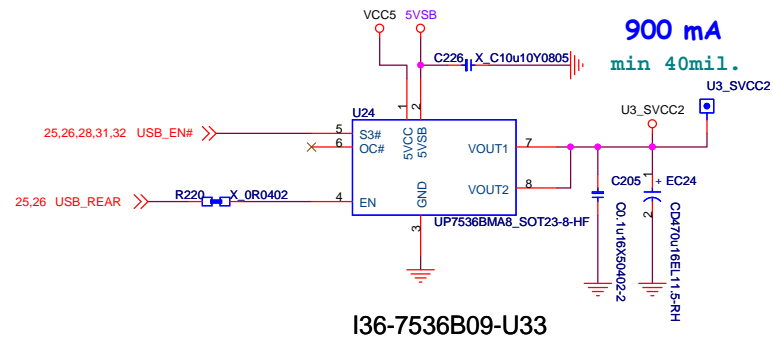


**MICRO-STAR INTL CO.,LTD**

**MS-7785**

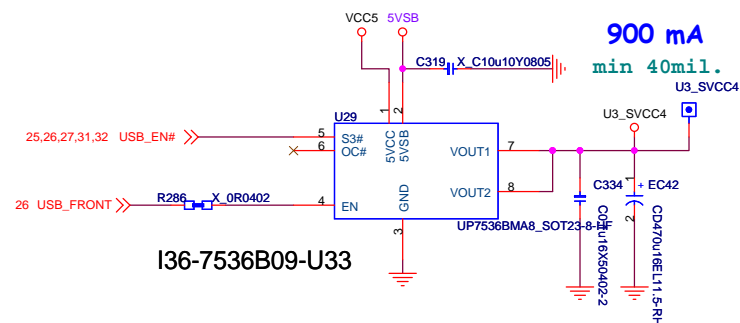
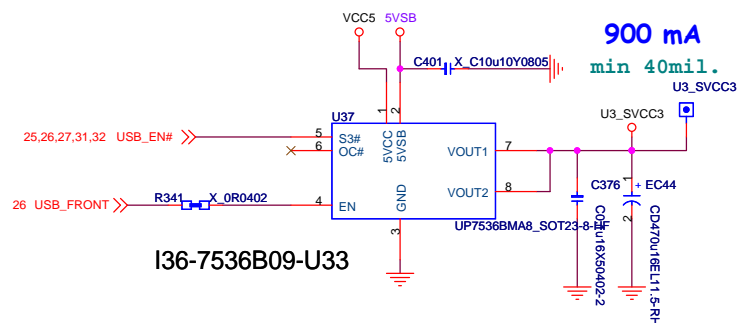
Size	Document Description	Rev
	<b>Front USB Connectors/ power</b>	<b>11</b>
Date:	Wednesday, March 14, 2012	Sheet 26 of 45

## USB3.0 Power Control

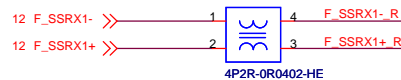
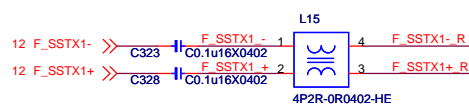
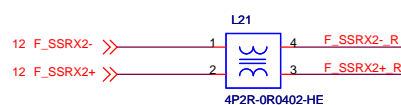
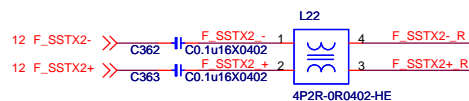
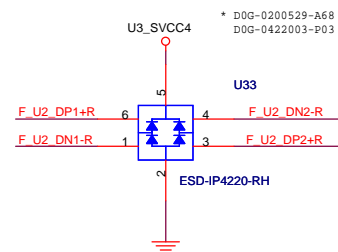
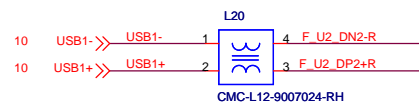
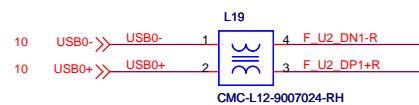
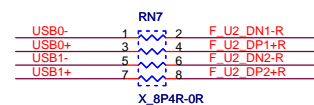


## Rear USB 3.0 ESD Protection

## USB3.0 Power Control



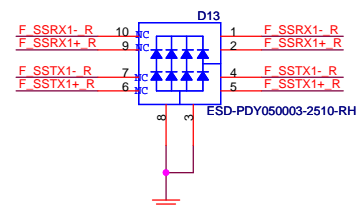
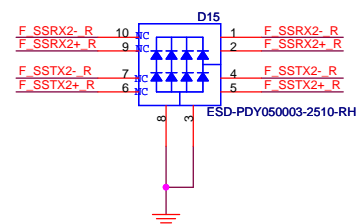
## USB 2.0 ESD Protection



CMC料號 : L12-9008050-N52  
0 ohm料號 : R3C-0000012-W08

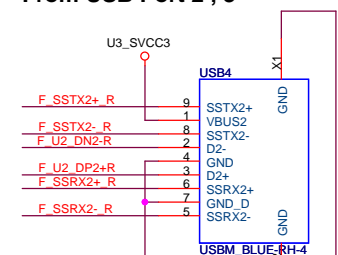
## Front USB 3.0 ESD Protection

(All component Near the connector)

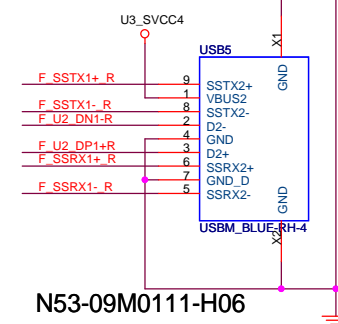


## CO-LAY

### Front Panel USB 3.0 Connector From USB Port 2 , 3



N53-09M0111-H06



直立式USB3.0 connector  
N53-09M0111-H06



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Size	Document Description <b>USB3.0-Front Port</b>	Rev <b>11</b>
Date:	Tuesday, March 13, 2012	Sheet 28 of 45

### 24 Pin ATX Power Connector



**POWER LED**

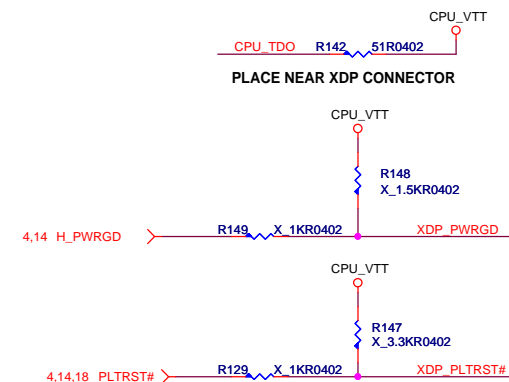
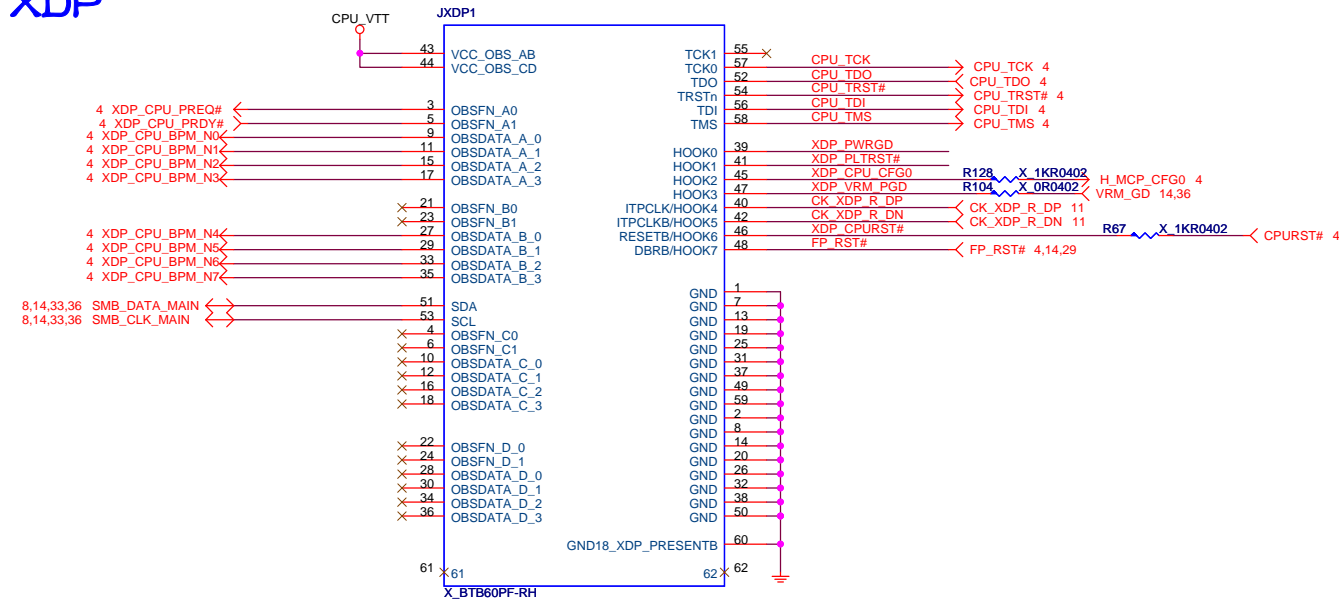


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Size	Document Description <b>ATX Connector / Front Panel / LED</b>	Rev <b>11</b>
Date:	Tuesday, March 13, 2012	Sheet 29 of 45

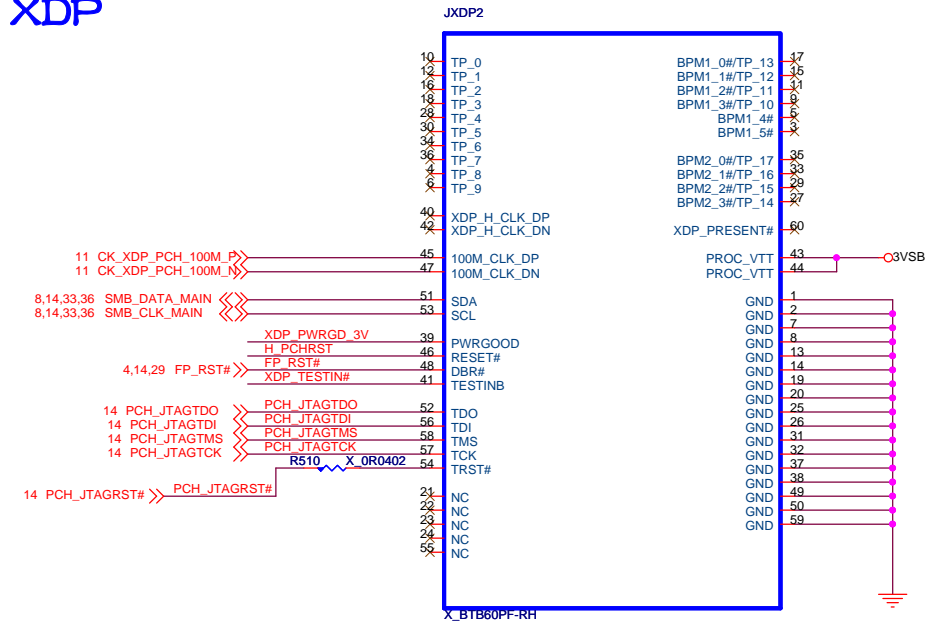


CPU  
XDP



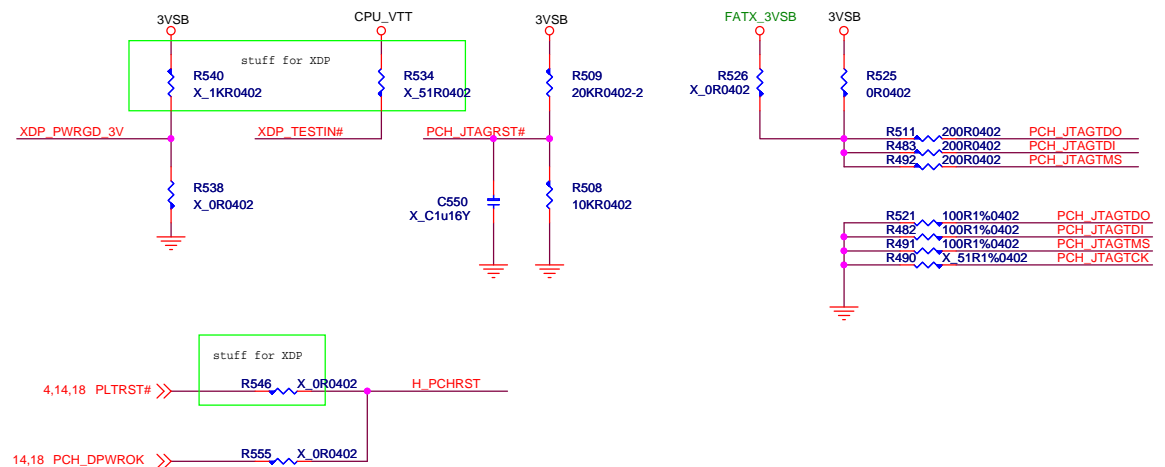
PCH  
XDP

N5C-60F0040-S88



N5C-60F0040-S88

## PCH XDP

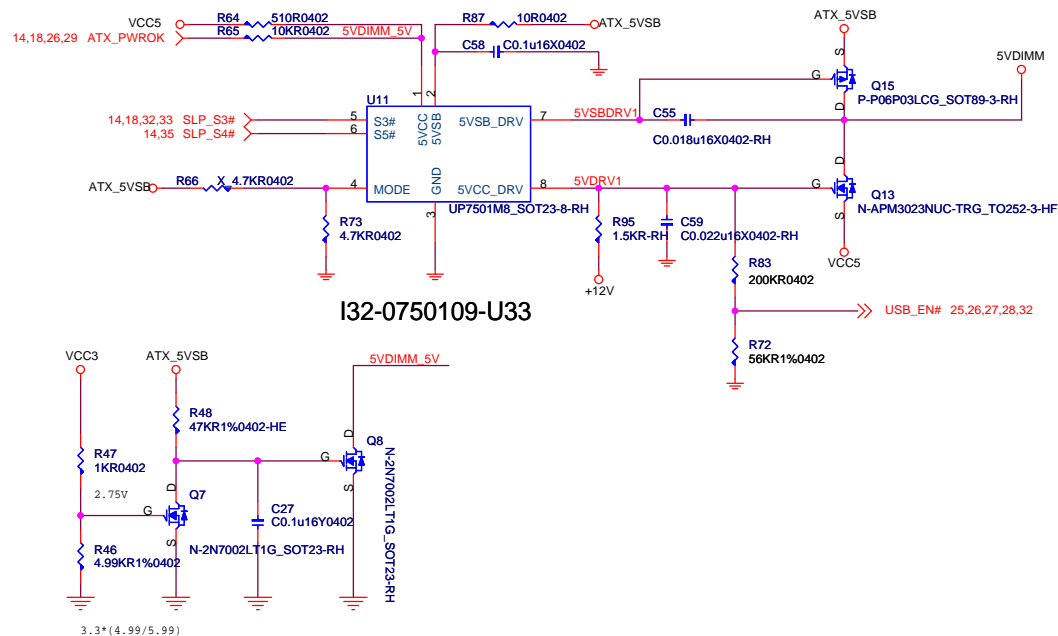


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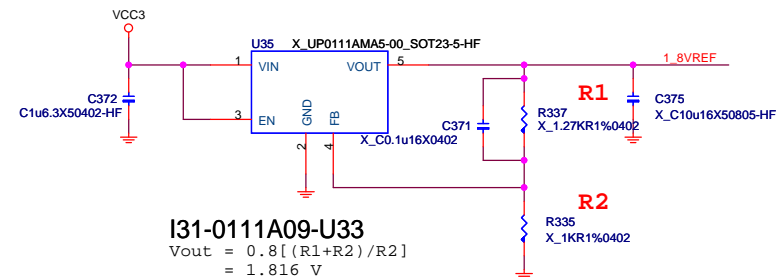
MS-7785

Size	Document Description <b>CPU/PCH XDP</b>	Rev <b>11</b>
Date:	Tuesday, March 13, 2012	Sheet 30 of 45

### **DDRIII Regulator Power Source**



### 1.8V Reference Power

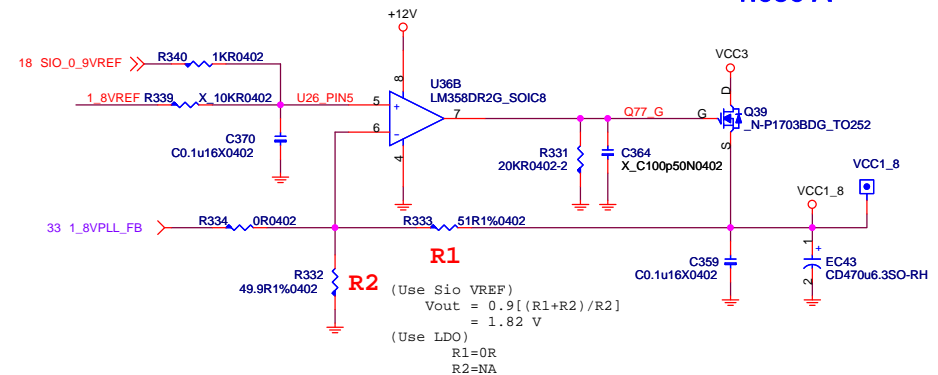


I31-0111A09-U33

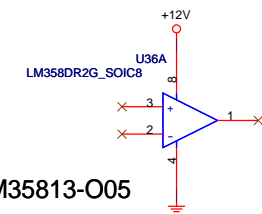
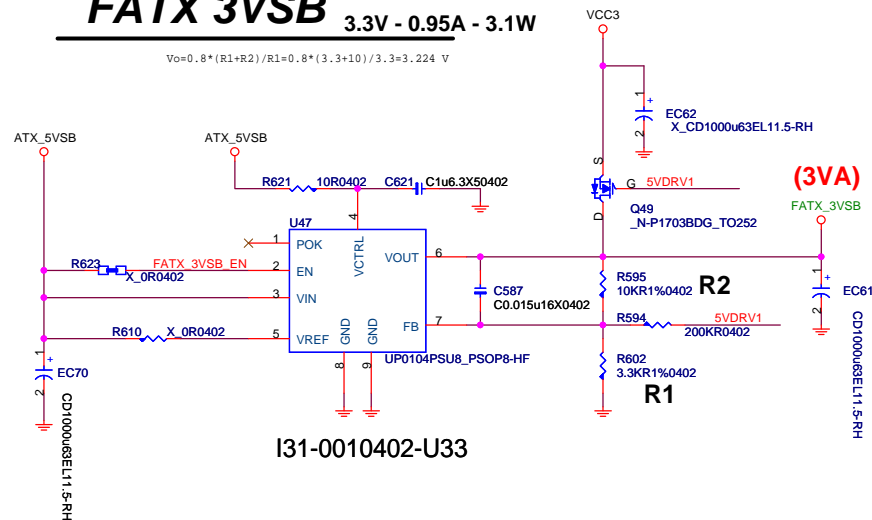
$$\begin{aligned} V_{out} &= 0.8[(R1+R2)/R2] \\ &= 1.816 \text{ V} \end{aligned}$$

$$\begin{aligned} V_{CC1\_8} &= V_{CCVRM} + V_{CCPLL} \\ &1.8 \text{ V} \\ &0.186 \text{ A} + 1.5 \text{ A} \\ &= 1.686 \text{ A} \end{aligned}$$

**1.8V VSFR**

**FATX 3VSB** 3.3V - 0.95A - 3.1W

$$V_O = 0.8 * (R_1 + R_2) / R_1 = 0.8 * (3.3 + 10) / 3.3 = 3.224 \text{ V}$$



I71-LM35813-O05



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**MS-7785**

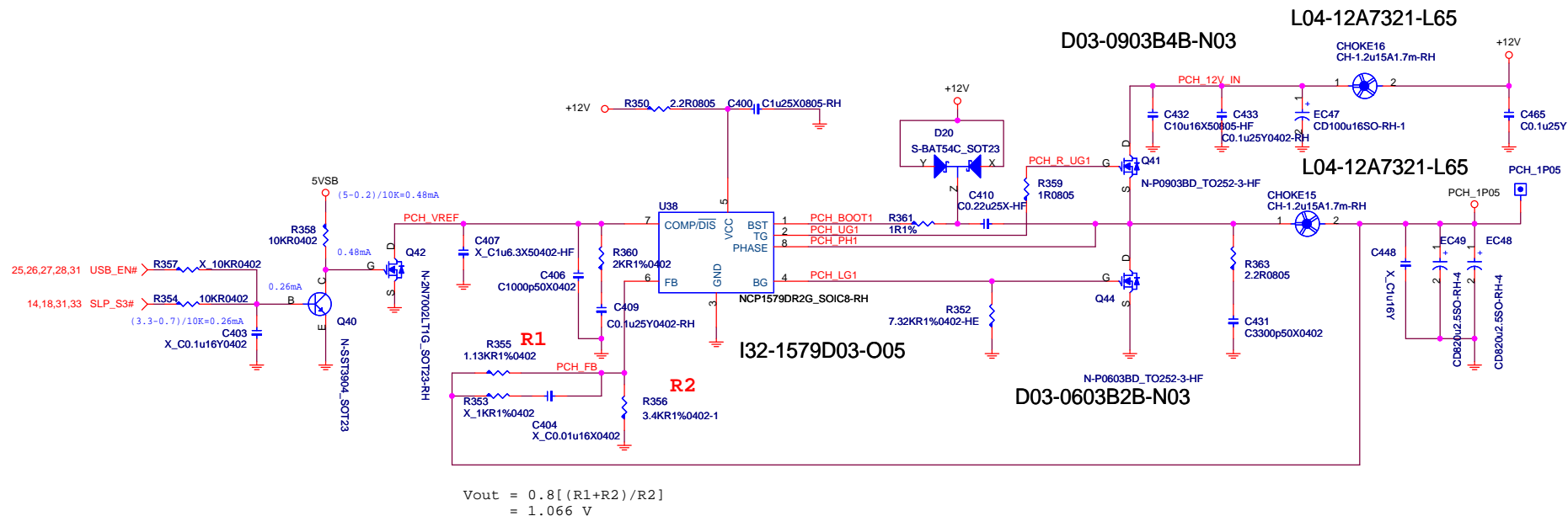
Size	Document Description	Rev
------	----------------------	-----

Size	Document Description	Rev
	<b>ACPI</b>	<b>11</b>

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PCH\_1P05  
1.05 V  
8.859 A  
OCP=16A

# PCH Core Power



EMI Resevr

PCH\_1P05

C466 X C0.1u16Y0402



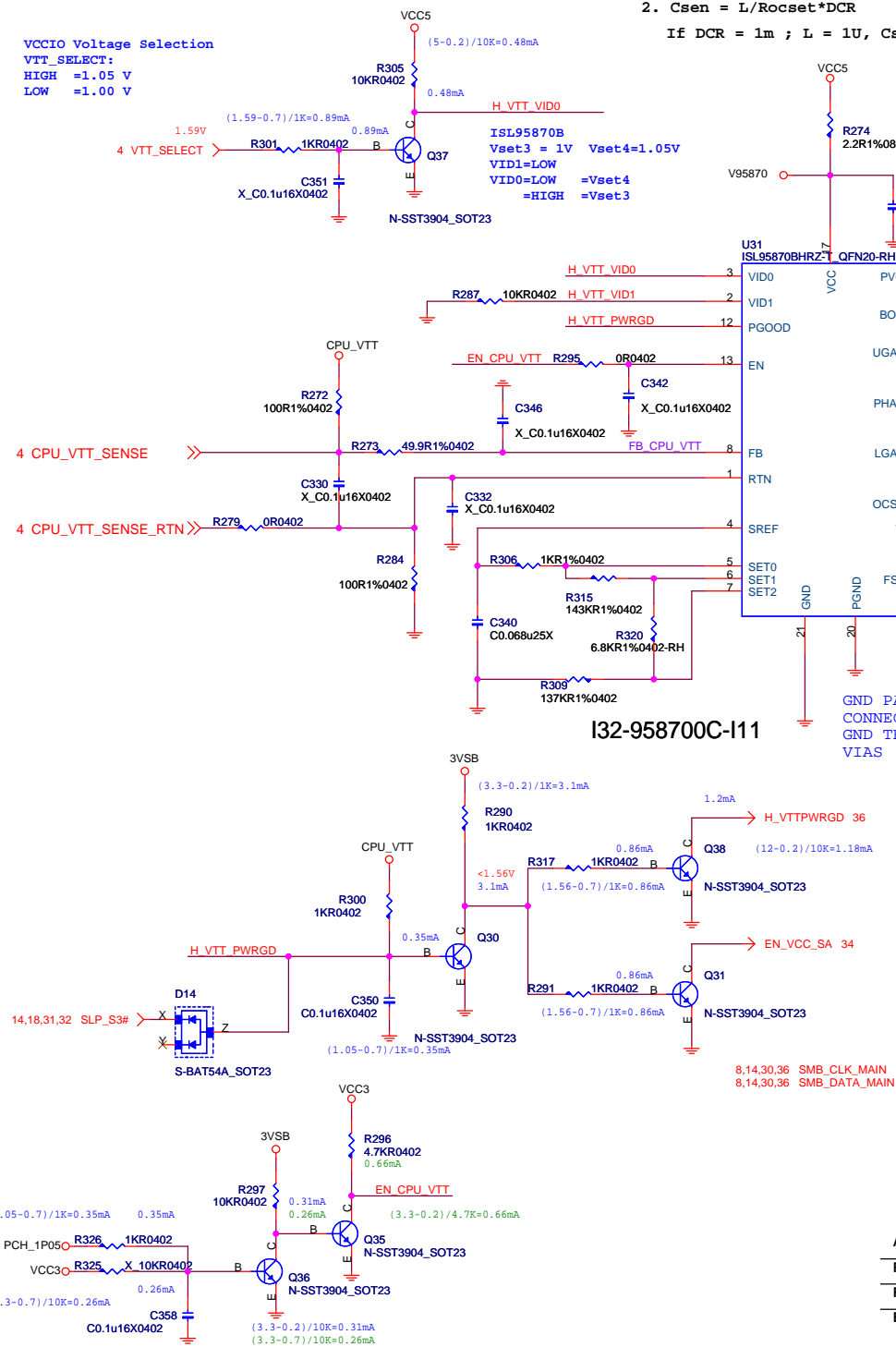
MICRO-STAR INTL CO.,LTD

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Size	Document Description	Rev
	PCH & ME Core Power	11
Date:	Wednesday, March 14, 2012	Sheet 32 of 45

### CPU VTT Power

```
VCCIO Voltage Selection
VTT_SELECT:
HIGH  =1.05 V
LOW   =1.00 V
```

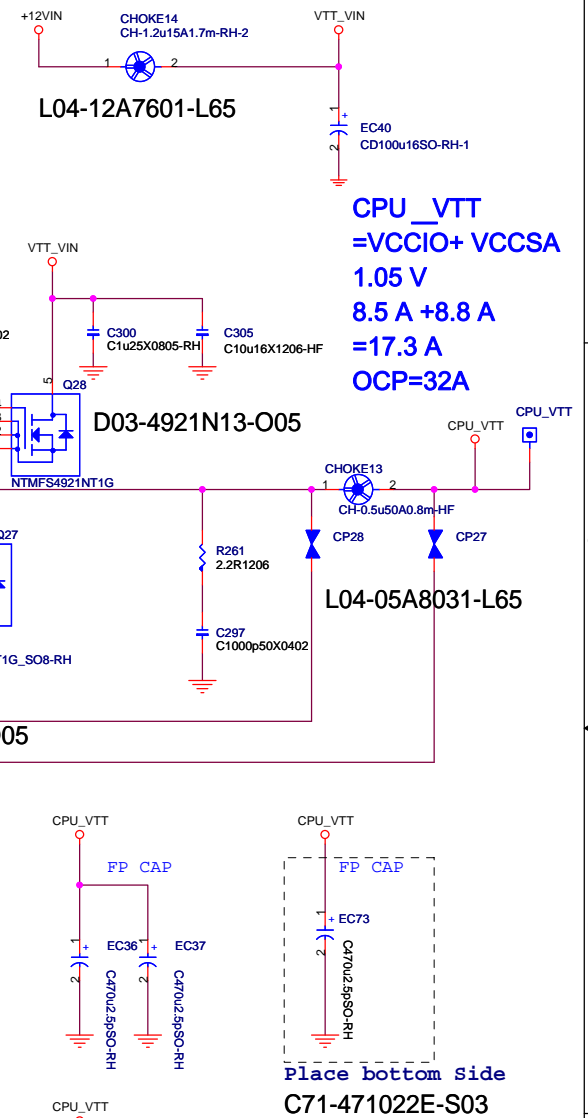


```

1. Rocset = Iout*DCR/Iocset ; Iocset = 10uA
   If DCR = 1m ; Iout = 20A, Rocset = 20A*1m/10uA --> Rocset = 2K

2. Csen = L/Rocset*DCR
   If DCR = 1m ; L = 1U, Csen = 1U/2K*1m --> Csen = 0.5U

```



## UPI VOLTAGE CONSOLE

ADDRESS	0x2A	0X28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%

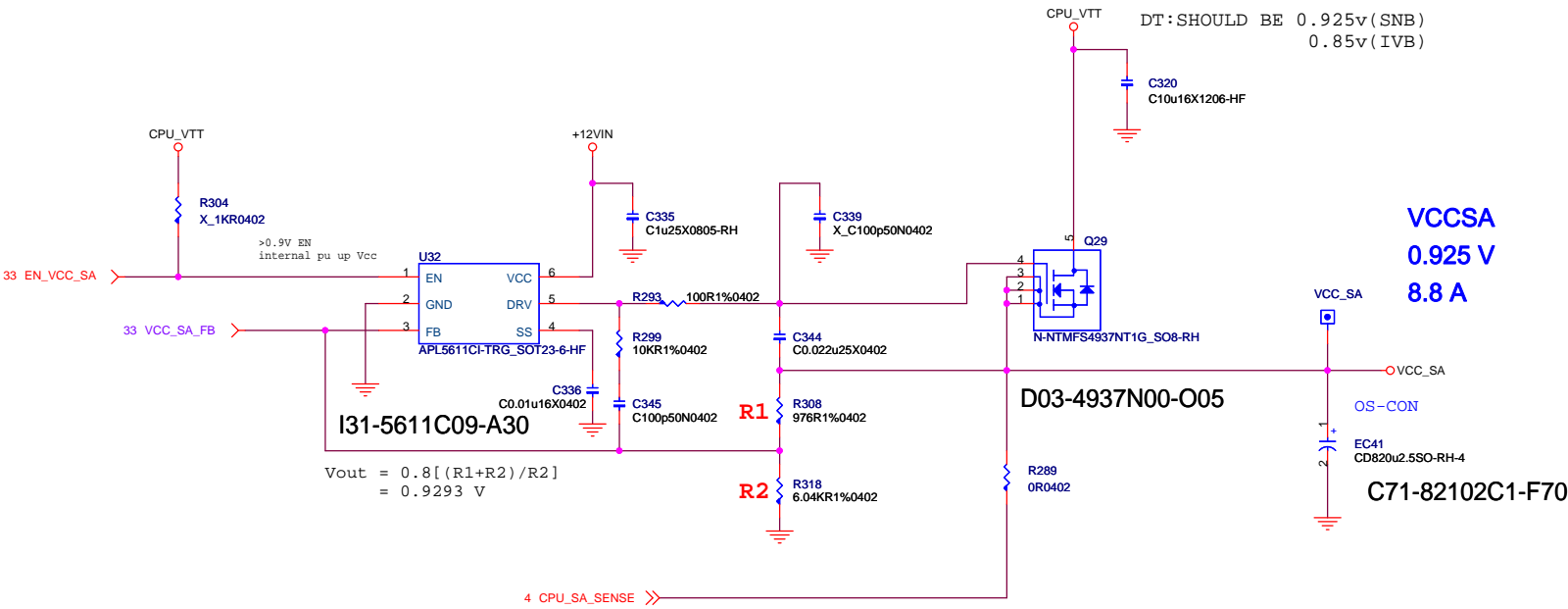


***MICRO-STAR INT'L CO.,LTD***

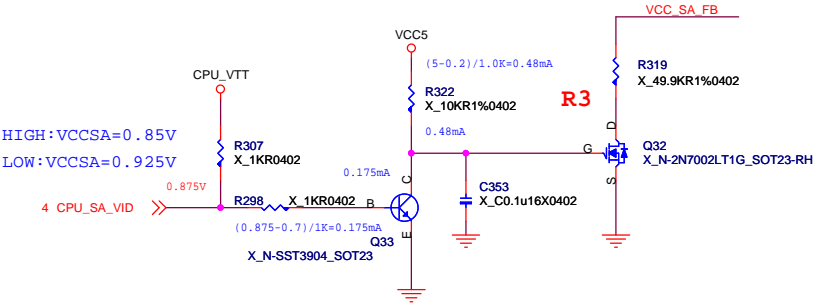
MS-7785

Size	Document Description <b>CPU VTT VR</b>	Rev <b>11</b>
Date:	Tuesday, March 13, 2012	Sheet 33 of 45

VCCSA



Reserved For CPU select SA\_VID  
R1= 1K  
R2= 13.7K  
R3= 11.8K

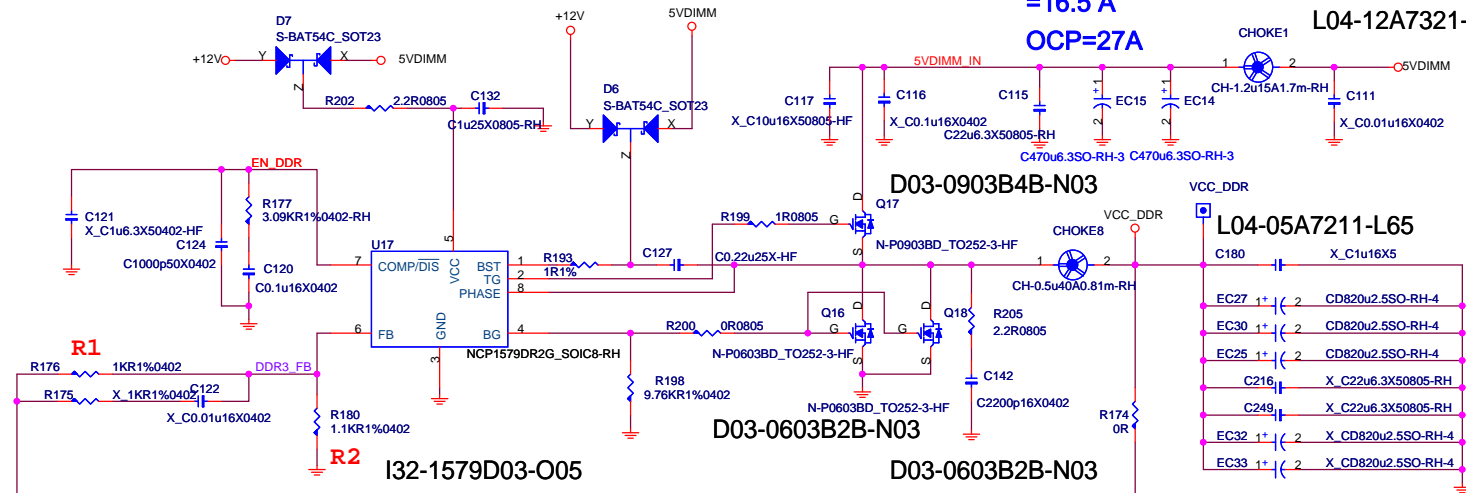


## DDRIII Power

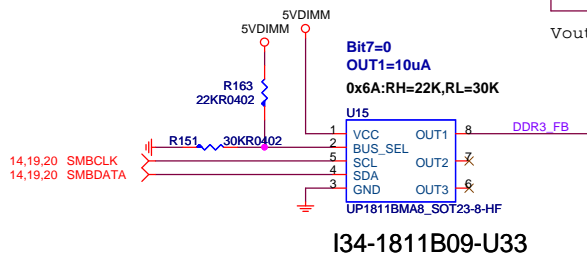
Iocp = Iocset\*Rocset/Rds(on) ; Iocset=10uA  
 L-MOS : D03-0603B2B-N03  
 = 10uA\*18.7K/2.9mohm = 64.5A  
 L-MOS: D03-0480600-005  
 = 10uA\*18.7K/4.7mohm = 39.8A

VCC\_DDR  
VDDQ+DDR POWER+VTT DDR  
1.5 V  
4.75 A +11 A+1 A  
=16.5 A  
OCP=27A

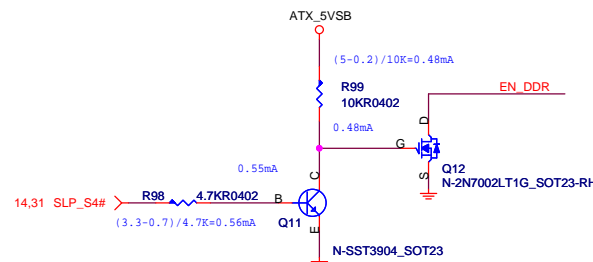
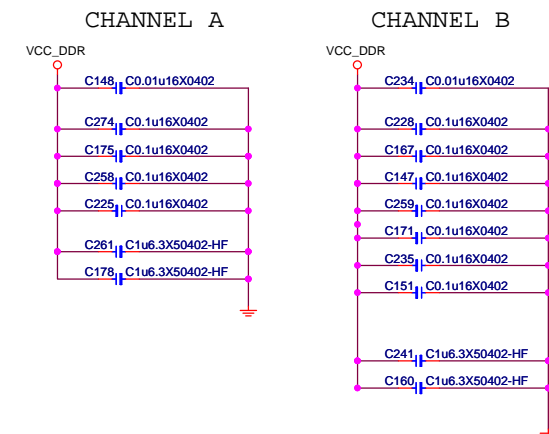
CHOKE1 L04-12A7321-L65



$$\begin{aligned} V_{out} &= 0.8[(R1+R2)/R2] \\ &= 1.527 \text{ V} \end{aligned}$$



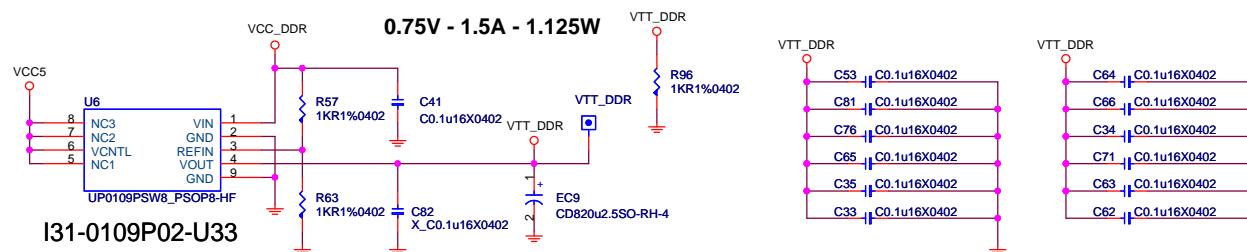
**DDRIII I/O power decoupling caps.**



## UPI VOLTAGE CONSOLE

ADDRESS	0x2A	0X28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%

### ***DDRIII Termination Power***



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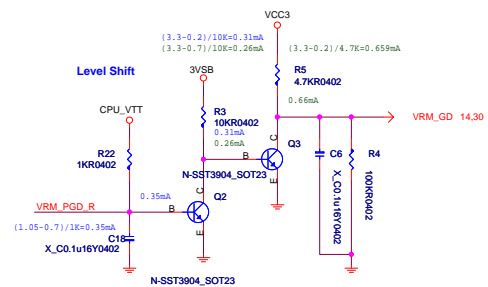
**MS-7785**

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	<b>DDR Power</b>	<b>11</b>
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## Voltage Regular Module (VRD12)

## ISL6366CRZ-T VRD12 POWER CKT

VCCP  
130A  
OCP=180A

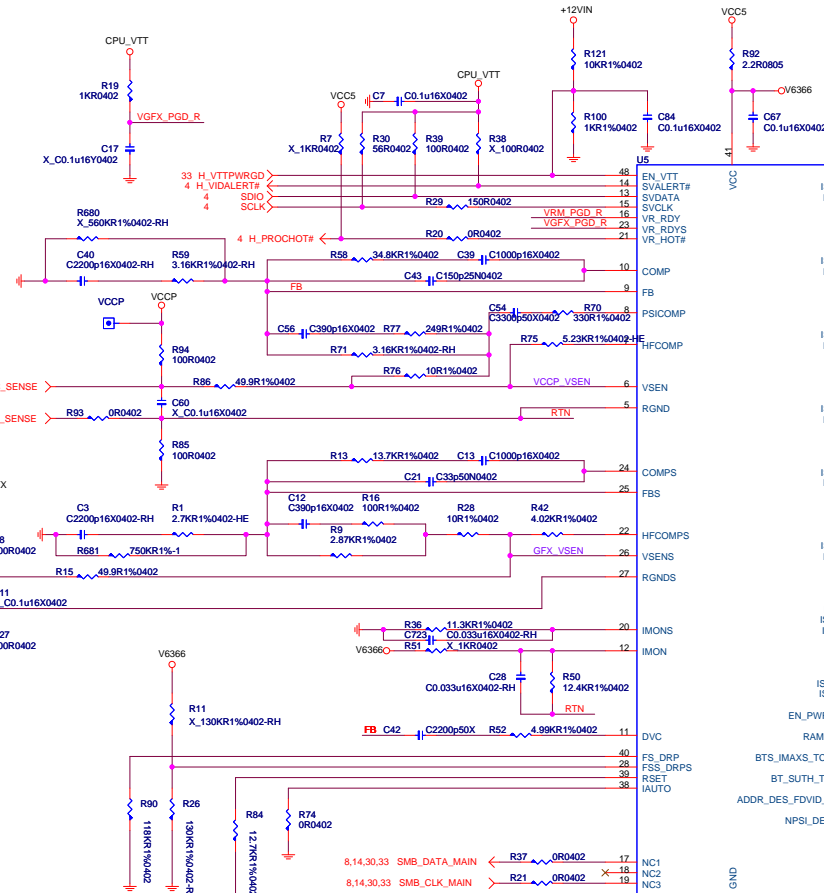
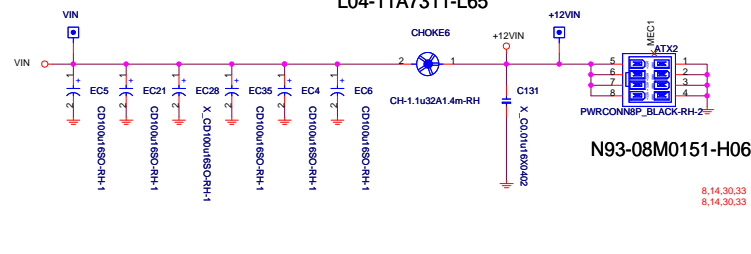


### 6366 6367 Option Table

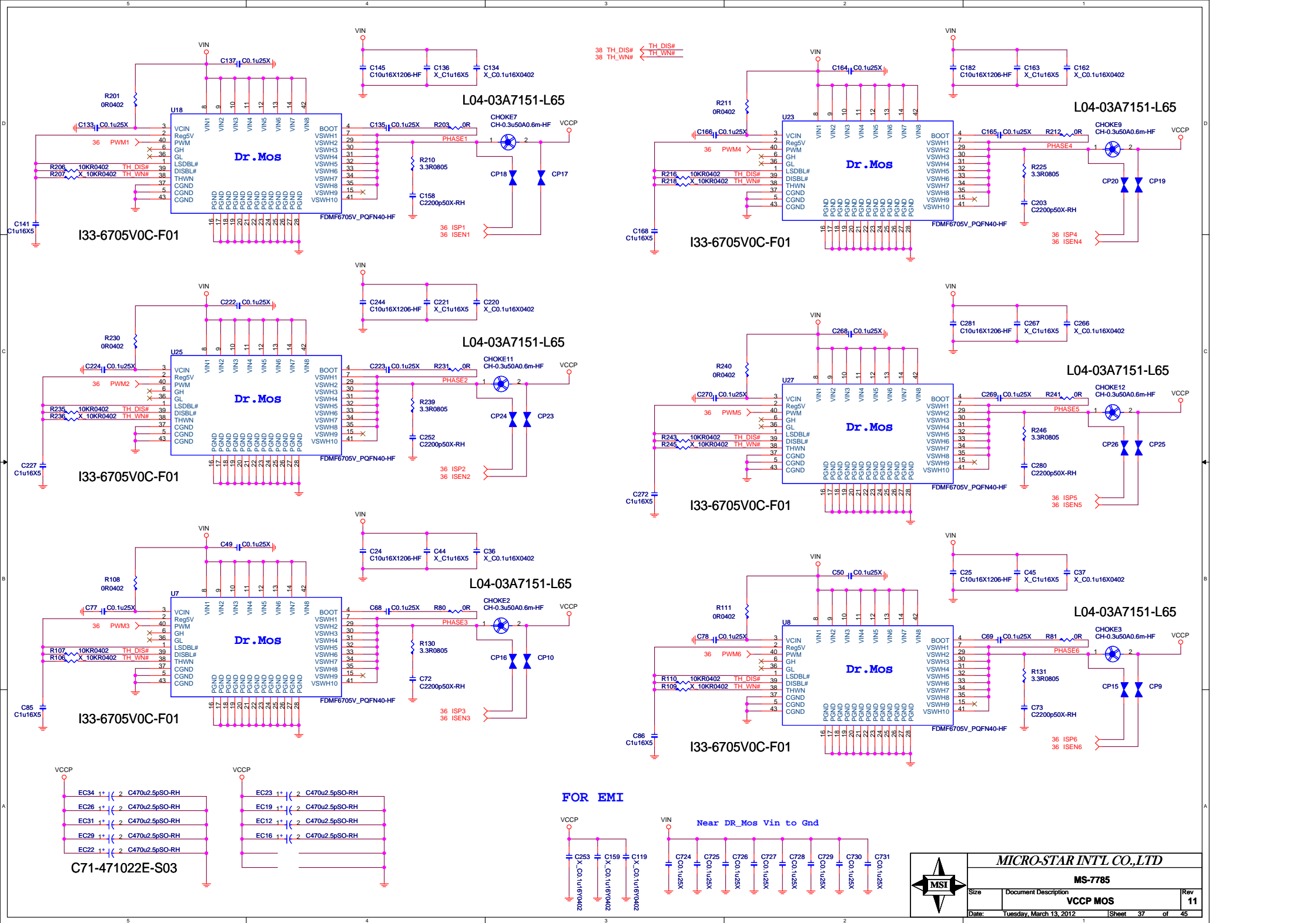
U5	R37	R21	R68	R69
6366 I32-6366C0C-I11	NC	NC	187K	453K
6367 I32-6367C0C-I11 PCB 1.0 Default Can use I2C to setting VCCP & +CPU_GFX Voltage and support Fix Mode	OR	OR	10K	NC

### CPU Core Power +12V Input

L04-11A7311-L65

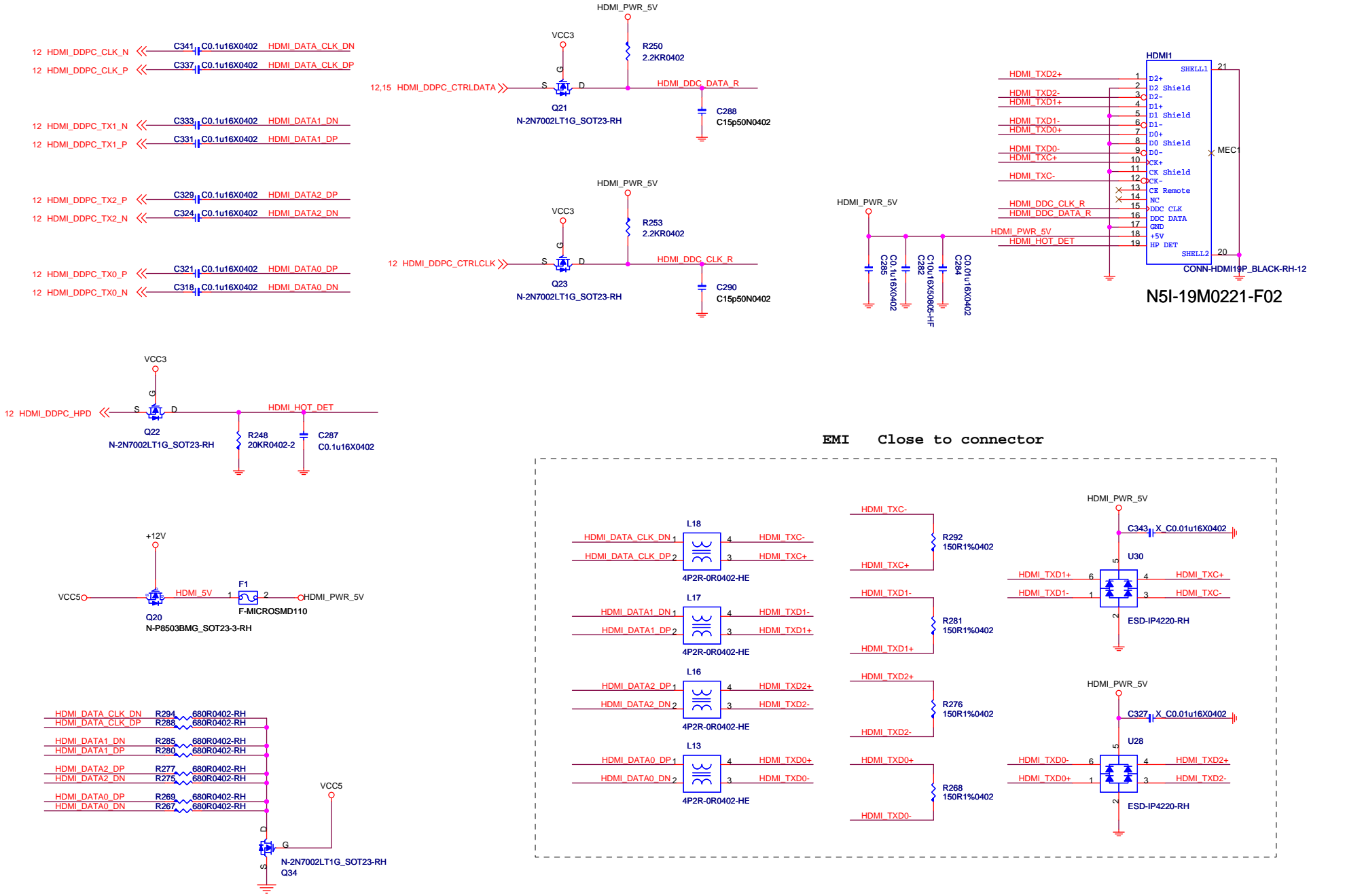


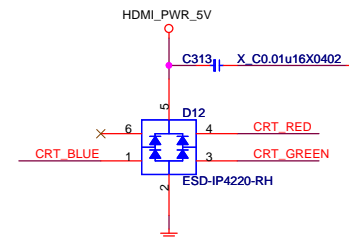
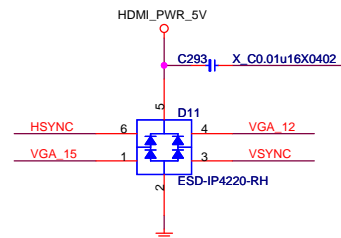
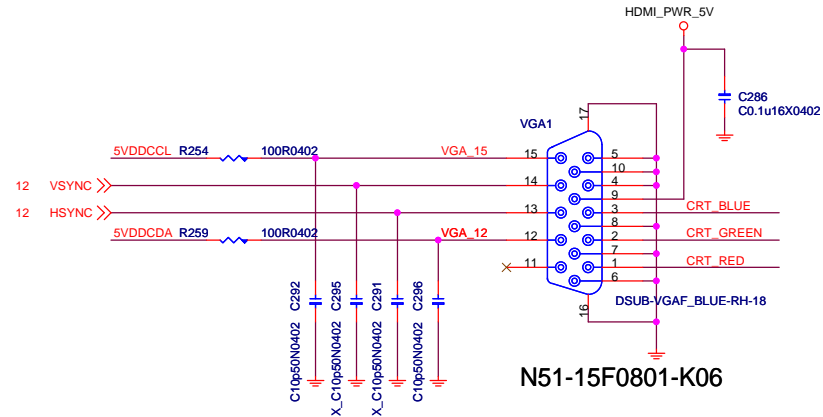
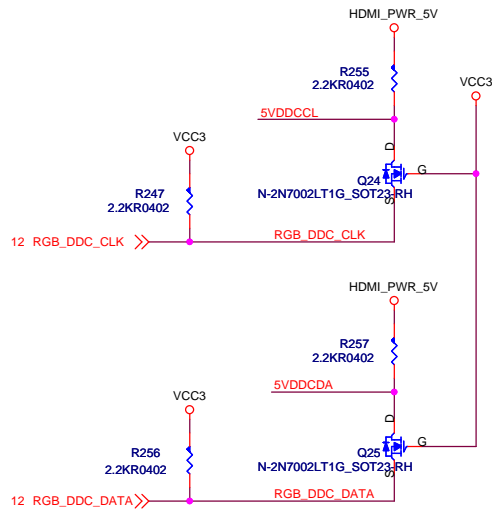
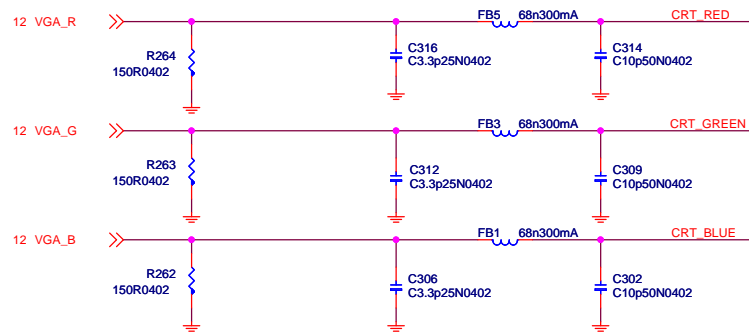






HDMI Connector



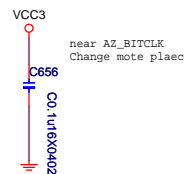
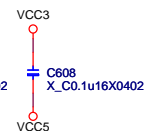
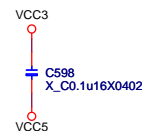
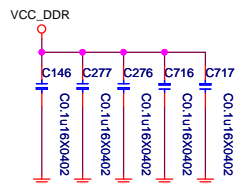
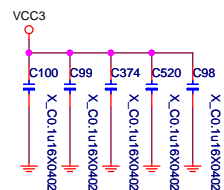
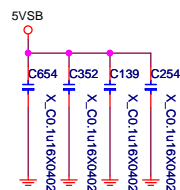
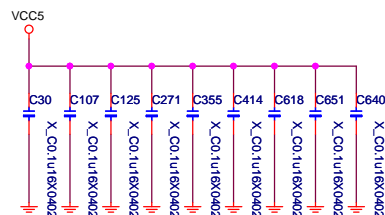
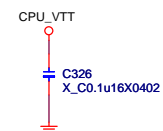
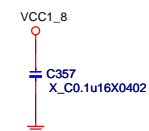
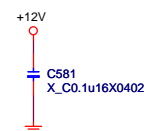
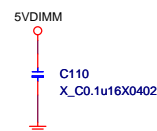
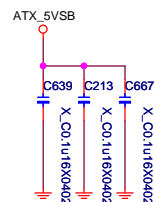
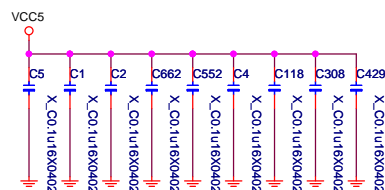


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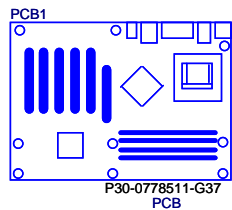
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# EMI CAPs

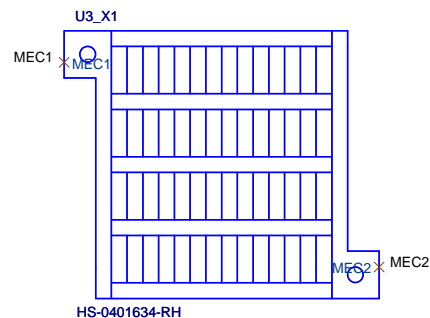
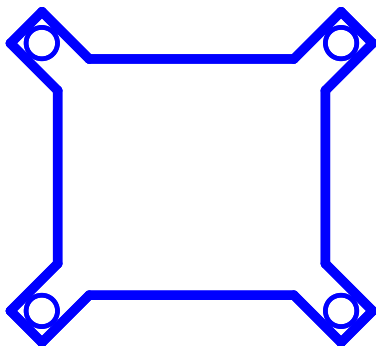


## Manual Parts



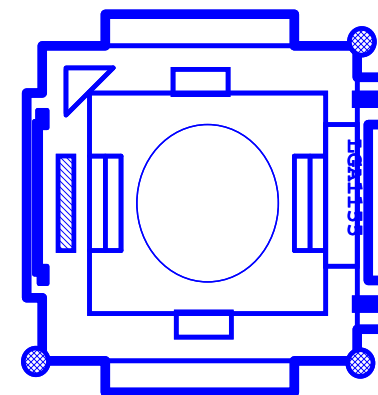
P30-0778511-G37  
P30-0778511-E48

XU1\_X2  
X\_CPU RETENTION BACKPLATE



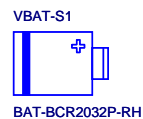
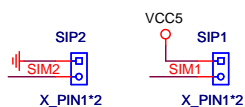
E31-0401634-K08

XU1\_X1  
CPU SOCKET



E21-7557060-F02

## Simulation



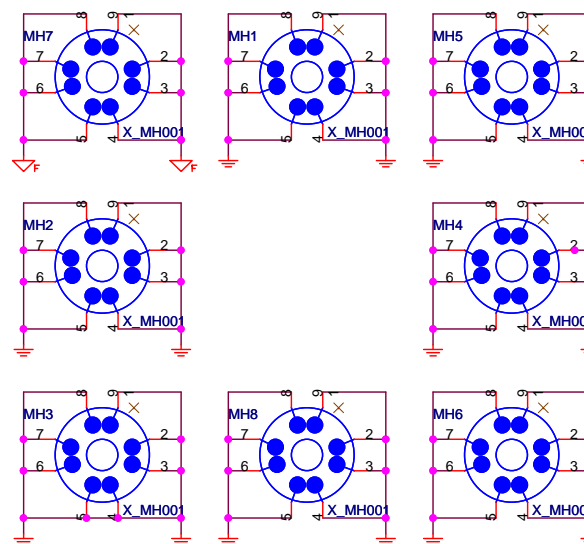
## HDMI VIRTUAL PN



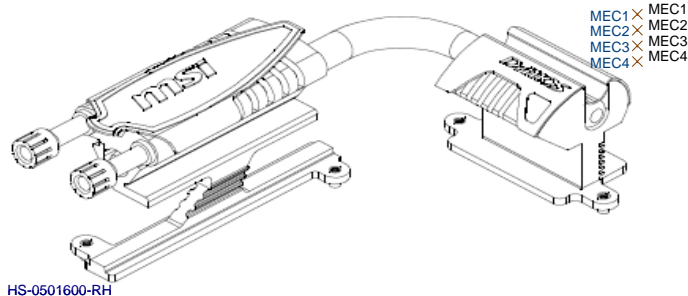
0.04 PER UNIT  
Y01-RHDMI03-000

## PCB Mounting Holes

### Mounting Holes



U21



E31-0501600-K08

LABEL1



G51-M1SPXXA-A09

LABEL2



G51-M1SPX33-Q13

## Optics Orientation Holes

### Optical Fiducial Marks-120



MICRO-STAR INTL CO.,LTD			
MS-7785			
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	Manual Parts & Option Parts		11
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